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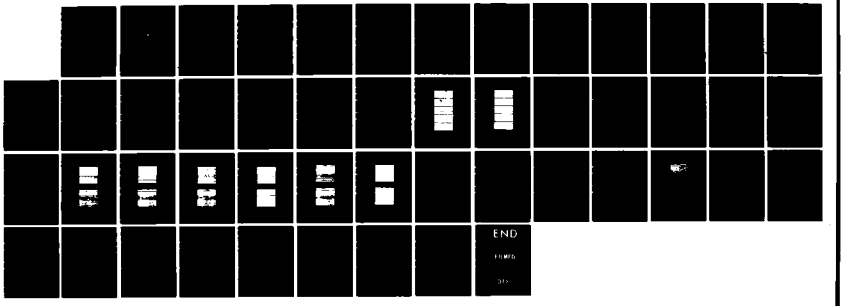

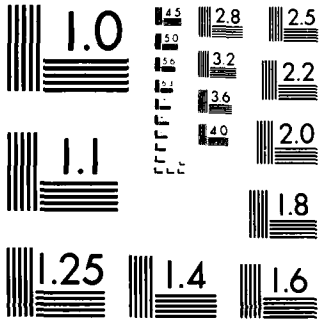

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THESIS

EXPERIMENTAL EVALUATION OF A NEW FORM OF M-ARY (M=8) PHASE SHIFT KEYING INCLUDING DESIGN OF THE TRANSMITTER AND RECEIVER

by

Gregory E. Thompson

December 1984

Thesis Advisor: G. A. Myers

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For transmitting digital information over bandpass channels, M-ary Phase Shift Keying (PSK) schemes are used to conserve bandwidth at the expense of signal power. A block of k bits is used to change the phase of the carrier. These k bits represent M possible phase shifts since $M = 2^k$. Common forms of M-ary PSK use equally spaced phase angles. For example, if M=8 and k=3, 8-ary PSK uses eight phase

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angles spaced 45 degrees apart.

This thesis considers a hybrid form of PSK when M=8 and k=3. Each of eight blocks of data with three bits per block are represented by different phase shifts of the carrier. The phase angles are chosen to give an equal distance between states (symbols) when projected onto the sine axis and the cosine axis of a phasor diagram. Thus, when the three bits are recovered, using two coherent phase detectors, the separation of the decision regions (voltage levels) are equal. This scheme was evaluated by building a transmitter and receiver to implement this 8-ary PSK technique. This method was found to improve the noise performance over conventional 8-ary PSK schemes by approximately 0.4 dB.

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Experimental Evaluation of a New Form of M-ary (M=8) Phase Shift Keying Including Design of the Transmitter and Receiver

by

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Major, United States Marine Corps
B.A., Concordia College, Moorhead, Minnesota, 1977

Submitted in partial fulfillment of the requirements for the degree of

MASTER OF SCIENCE IN ELECTRICAL ENGINEERING

from the

NAVAL POSTGRADUATE SCHOOL
December 1984

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ABSTRACT

For transmitting digital information over bandpass channels, M-ary Phase Shift Keying (PSK) schemes are used to conserve bandwidth at the expense of signal power. A block of k bits is used to change the phase of the carrier. These k bits represent M possible phase shifts since $M = 2^K$. Common forms of M-ary PSK use equally spaced phase angles. For example, if M=8 and k=3, 8-ary PSK uses eight phase angles spaced 45 degrees apart.

This thesis considers a hybrid form of PSK when M=8 and k=3. Each of eight blocks of data with three bits per block are represented by different phase shifts of the carrier. The phase angles are chosen to give an equal distance between states (symbols) when projected onto the sine axis and the cosine axis of a phasor diagram. Thus, when the three bits are recovered, using two coherent phase detectors, the separation of the decision regions (voltage levels) are equal. This scheme was evaluated by building a transmitter and a receiver to implement this 8-ary PSK technique. This method was found to improve the noise performance over conventional 8-ary PSK schemes by approximately 0.4 dB.

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LIST OF FIGURES

I. INTRODUCTION

A. BACKGROUND

Today, there is an increasing demand for high-speed digital communications systems. This demand comes at a time of decreasing available radio frequency (RF) spectrum. Therefore the development of bandwidth efficient, low probability of error, digital modulation schemes becomes increasingly important.

M-ary digital modulation schemes provide a means of conserving bandwidth at the expense of increased power requirements. Thus, M-ary digital modulation schemes can be used to achieve higher data rates in a given bandwidth. In an M-ary modulation system, one of M possible symbols is transmitted during a signaling interval. Each symbol represents a block of k data bits where $M = 2^k$. Each symbol in the M-ary modulation scheme is identifiable by its phase, amplitude, or frequency, or a combination of these three. At the receiver, the symbol is identified and decoded into a block of k data bits.

B. PHASE SHIFT KEYING

The subject of this report is 8-ary Phase Shift Keying (PSK). This is defined as a carrier of fixed frequency, fixed amplitude, and eight different phase angles. Figure 1.1 is a phasor diagram for conventional PSK. Note that the phasors are spaced by 45 degrees. During recovery of conventional PSK, in-phase (cosine) and quadrature (sine) phase detectors are used with appropriate threshold detectors and logic. The output of each phase detector is the cosine or the sine of the phase angle of the received signal.

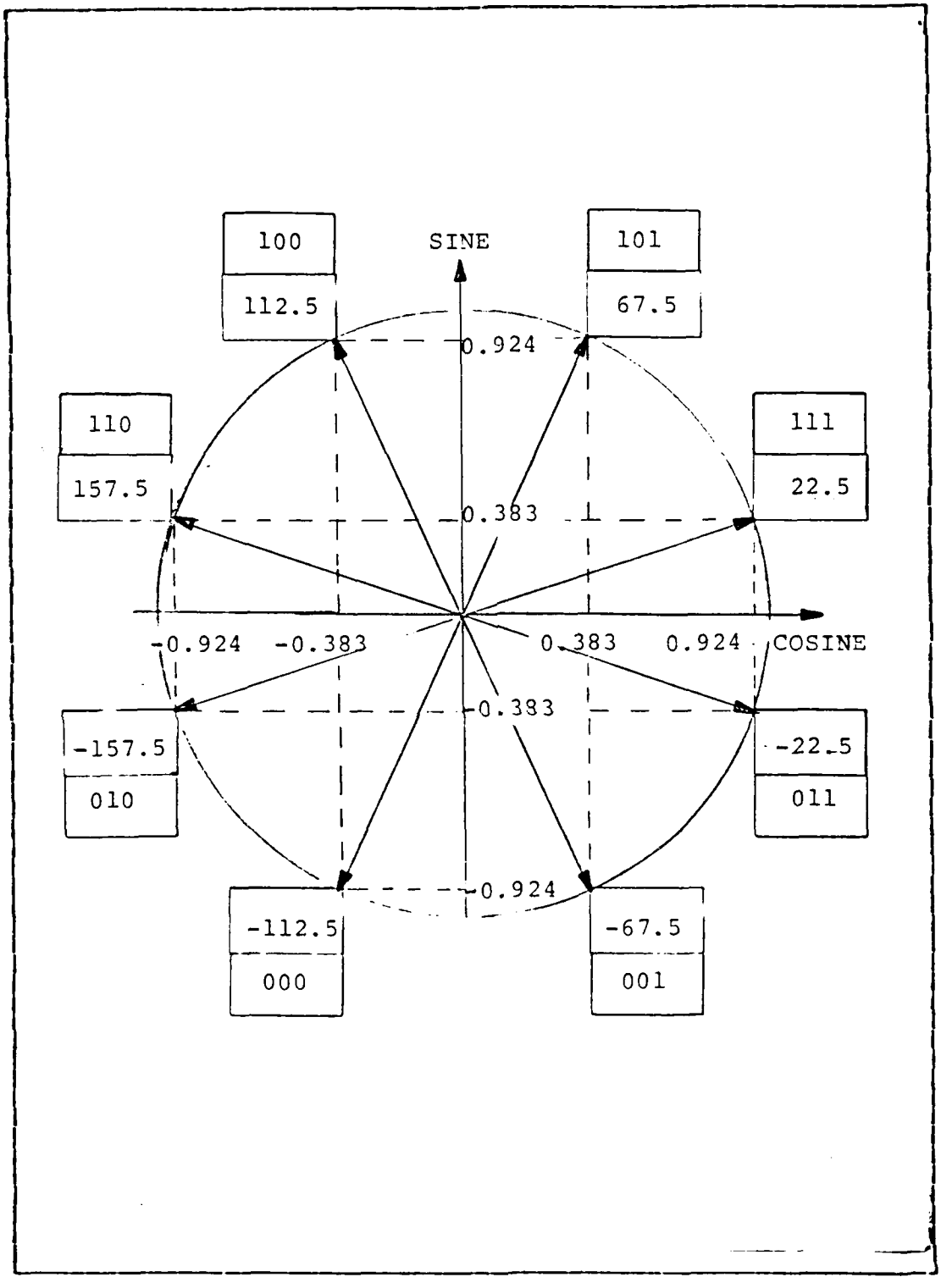

Figure 1.1 Phasor Diagram for Conventional PSK (M=8)

This output is a voltage that can be processed to recover the bits originally sent by the transmitter. Figure 1.1 shows these voltage values assuming the circle has a radius of one. Note that the voltages, which determine the decision regions, are not separated equally. If a system is built where these decision regions (voltages) are spaced equally, it is reasonable to expect better noise performance. This report examines a communications system built using a new modulation scheme which accomplishes this.

C. A NEW MODULATION TECHNIQUE

The communications system built to incorporate this new modulation technique consists of a transmitter and a receiver. The transmitter selects one of eight shifted carriers corresponding to eight different symbols and transmits it to the receiver.

In the receiver, in-phase and quadrature phase detectors are used with appropriate threshold detectors and logic to recover the eight symbols.

Decision theory states for minimum error [Ref. 4], decision regions should be spaced equally. Since a decision is made based on a certain voltage level (and not on phase), it is reasonable to select phase angles which provide equal separation of voltage levels out of the phase detectors. For example, in Fig. 1.1, although the phases are spaced equally, the decision regions (voltages) are not.

The solution to accomplishing this can be found using simple algebra. Figure 1.2 is a phasor diagram of the 8-ary PSK used in this discussion. Note that the decision regions are equally separated. The reason, then, for the selection of this method under study is for improved noise performance over conventional techniques.

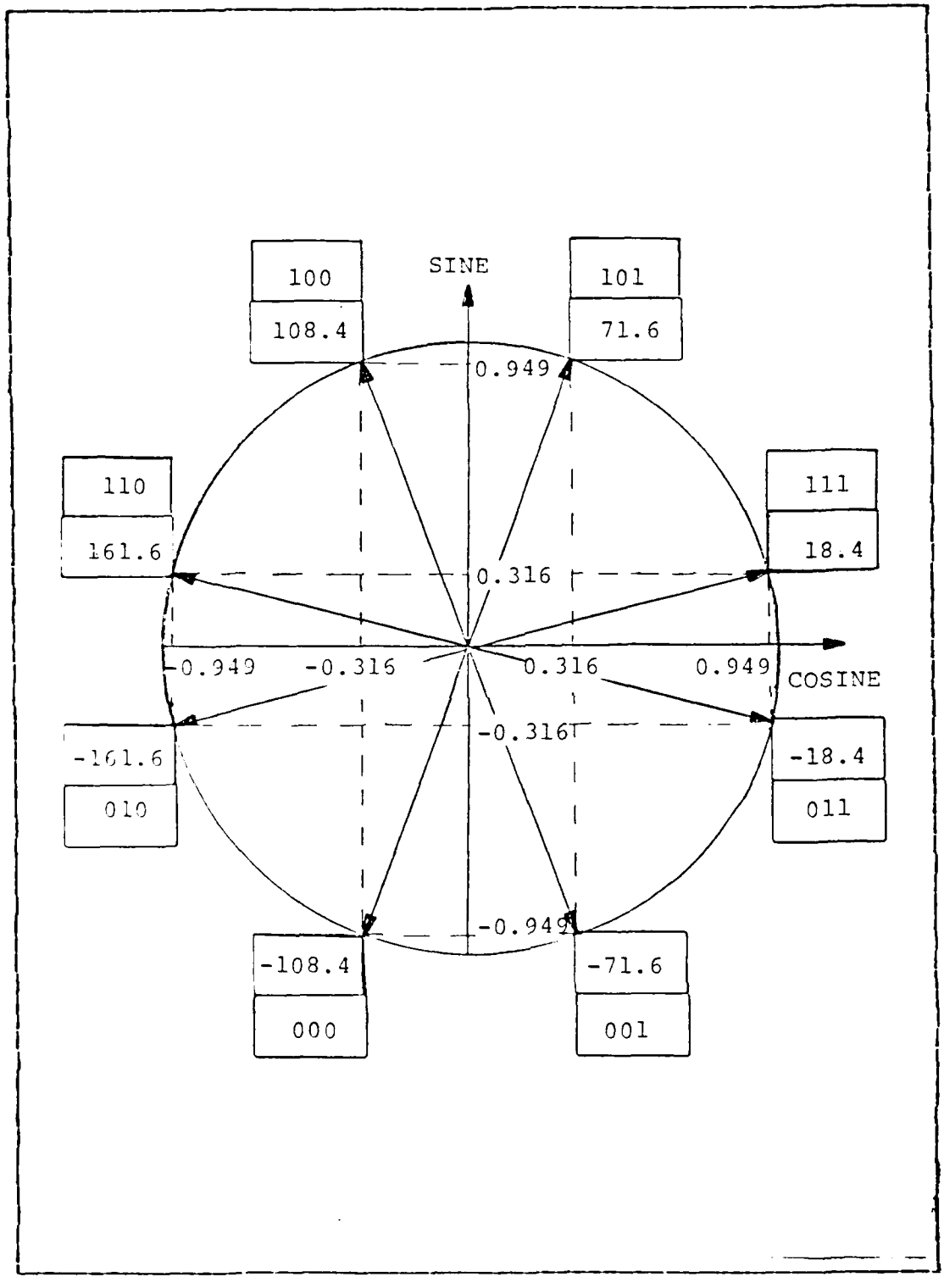

Figure 1.2 Phasor Diagram for NEW PSK (M=8) Method

the least significant bit and the middle bit in branch #1 and equation 3.4 is used to recover the most significant bit in branch #2.

$$(\cos(\omega t))(\cos(\omega t+\theta)) = 1/2(\cos(2\omega t+\theta)+\cos\theta) \qquad \text{(eqn 3.1)}$$

$$(\sin(\omega t))(\cos(\omega t+\theta)) = 1/2(\sin(2\omega t+\theta)+\sin(-\theta)) \qquad \text{(eqn 3.2)}$$

$$1/2\cos(\theta) \qquad \text{(eqn 3.3)}$$

$$1/2\sin(-\theta) \qquad \text{(eqn 3.4)}$$

Figures 3.3, 3.4, 3.5, and 3.6 show photographs of the output of the phase detectors of branches #1 and #2, respectively.

A decision is based on the polarity of the voltages, namely, logical one for a positive voltage and logical zero for a negative voltage. The gain factor of the amplifier is controlled by a potentiometer in the feedback loop. This allows the output voltage level of the phase detector for phase angles 71.6 , 108.4 , -71.6 , -108.4 (low value) to be less than one. This is desirable because in the circuit for the recovery of the middle bit the AVM is used as a squarer. Thus, the low magnitude voltage is made relatively smaller and the high magnitude voltage is made relatively larger. A decision is based on the difference in magnitude of the squares of the voltages corresponding to four phase angles and the other four phase angles 18.4 , 161.6 , -18.4 , and -161.6 . The photographs of the output of the squarer amplifier are shown in Figures 3.7 and 3.8 and the detailed circuitry of the phase detector is shown in Figure 3.9. The photographs of the output of the squarer show a negative voltage for two of the cases. This is acheived by biasing the AVM and the procedure for this is explained in Section III. C.

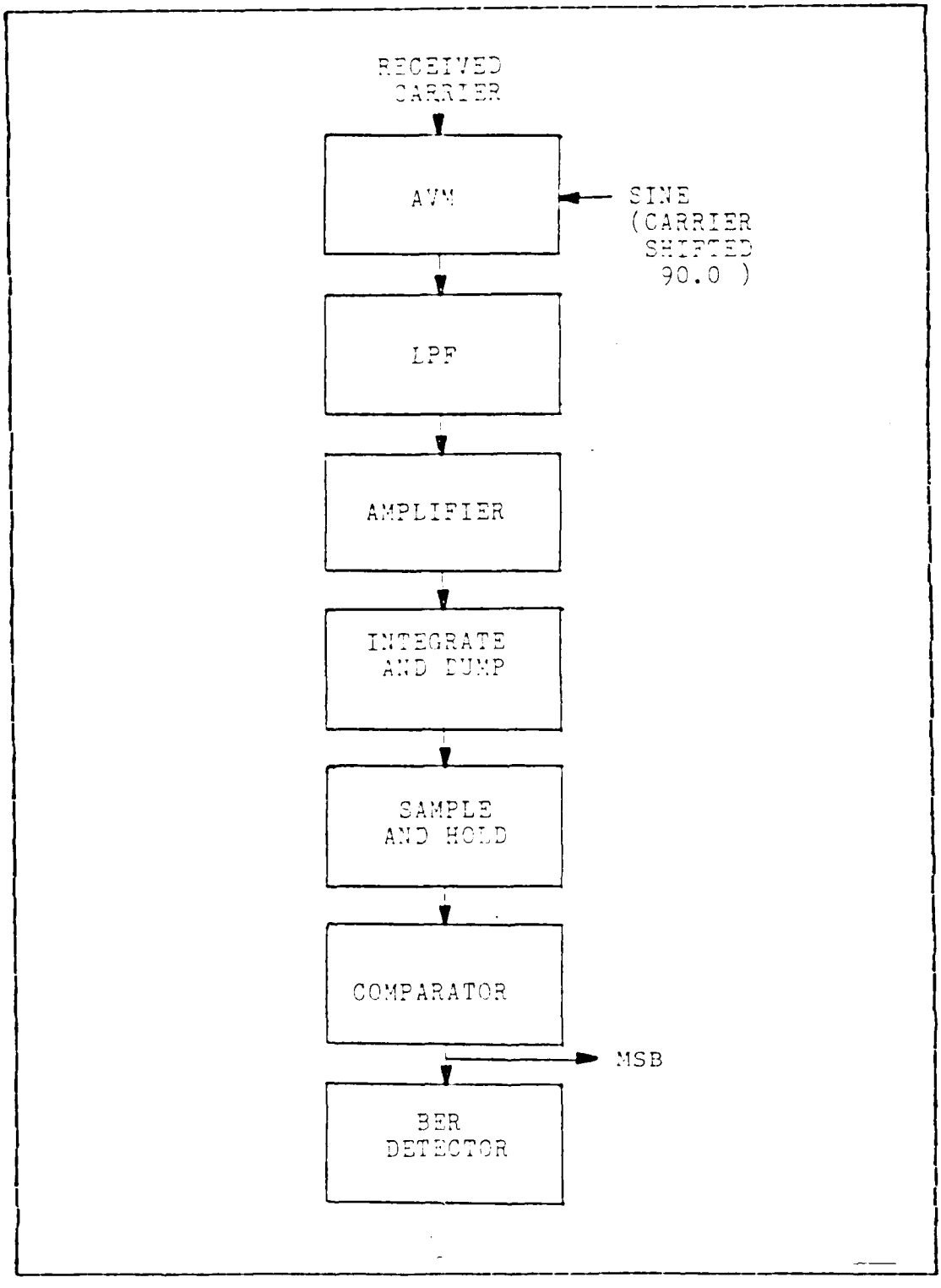

Figure 3.2 Block Diagram of Branch #2 for Recovery of MSB

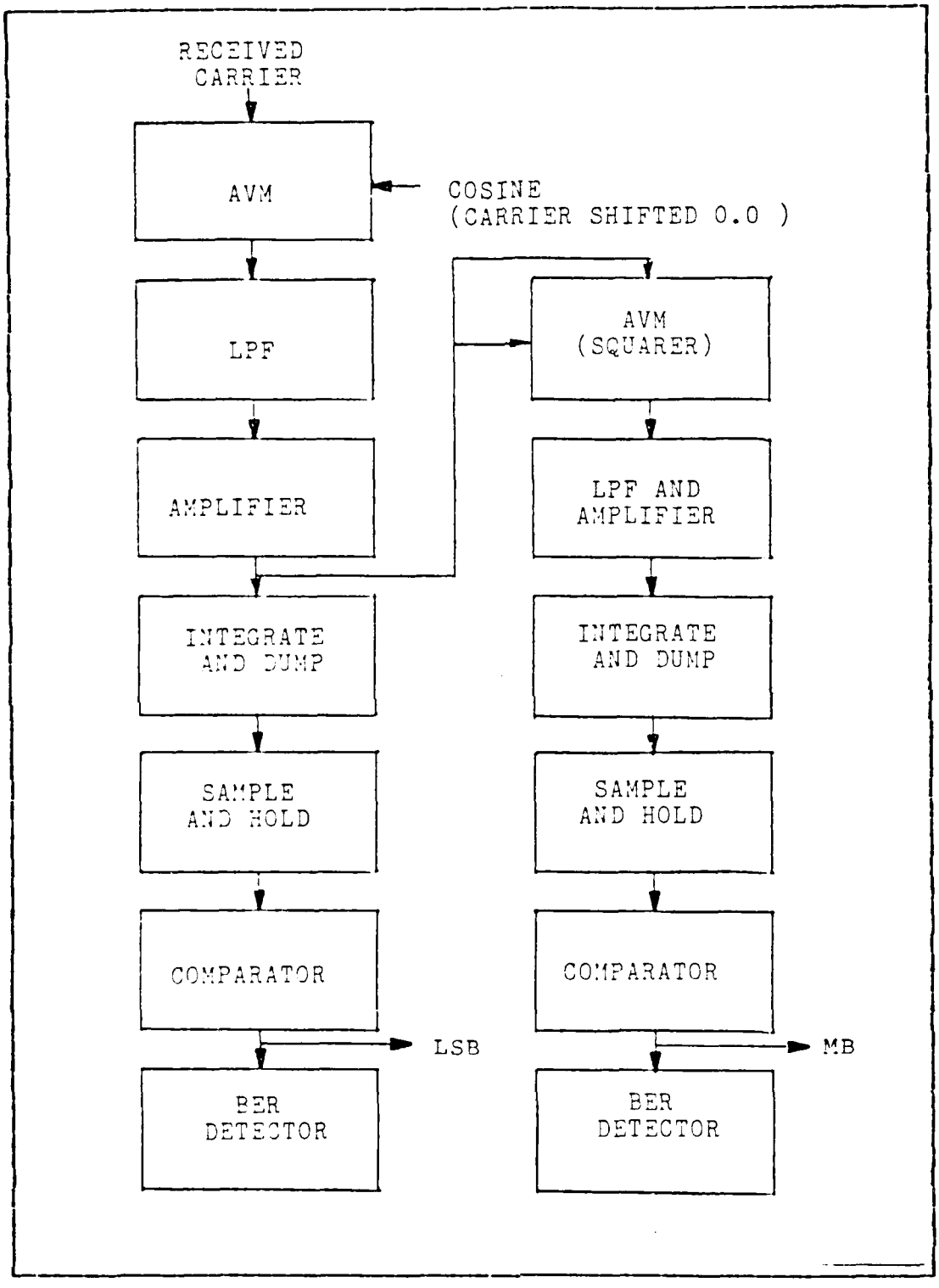

Figure 3.1 Block Diagram of Branch #1 for Recovery of LSB & MB

III. RECEIVER

The receiver consists of two branches. The first branch (Figure 3.1) is used to recover the least significant bit (LSB) and the middle bit (MB). The second branch (Figure 3.2) is used to recover the most significant bit (MSB). From the figures it can be seen that the least and most significant bits are recovered in exactly the same way. The only difference is the choice of the cosine or sine reference signal. The logical one or zero is determined by the polarity of the output of the analog voltage multiplier (AVM). The middle bit is determined by the magnitude of the output of the AVM of branch #1. The AVM is used to form the square of those voltage values on the cosine axis of Figure 1.2. This squaring maps ± 0.949 values into one voltage level and ± 0.316 values into another voltage level. These two levels represent the middle bit. Further, squaring increases the separation of the two levels and improves the noise performance of the middle bit recovery process.

A. PHASE DETECTOR

The phase detector is composed of an AVM, low pass filter (LPF), and an amplifier. The basic element used to detect the phase is the AVM. The one selected for this circuit is the AD 534. The output of the AVM is the product of the modulated carrier and the reference sinusoid. This output is scaled (reduced) by a factor of ten. This factor of ten is compensated for by the amplifier of this stage. The results of the product operations are given in equations 3.1 and 3.2. The double frequency terms are removed by the low pass filter. The resulting usable outputs are given in equations 3.3 and 3.4. Equation 3.3 is used to recover

Gray Coding. Figure 1.2 of the previous chapter is a phasor diagram showing each phasor with its three bit code. When an error occurs in transmission, the chosen symbol is most likely adjacent to the correct symbol (on phasor diagram). Since a symbol has three bits, then if a Gray code is used, at most one bit will be in error and two bits will be correct. In other words, the probability of a bit error is equal to the probability of a symbol error. The other significant feature of the coding scheme is that the least significant bit (LSB) is a logical one in the positive half of the cosine axis and a logical zero in the negative half. The most significant bit (MSB) is a logical one in the positive half of the sine axis and is a logical zero in the negative half. Furthermore, the middle bit (MB) is a logical one for the phasors whose absolute value on the cosine axis is largest and a logical zero for the smaller absolute value. These facts will aid in the recovery of each bit and is discussed further in Chapter III.

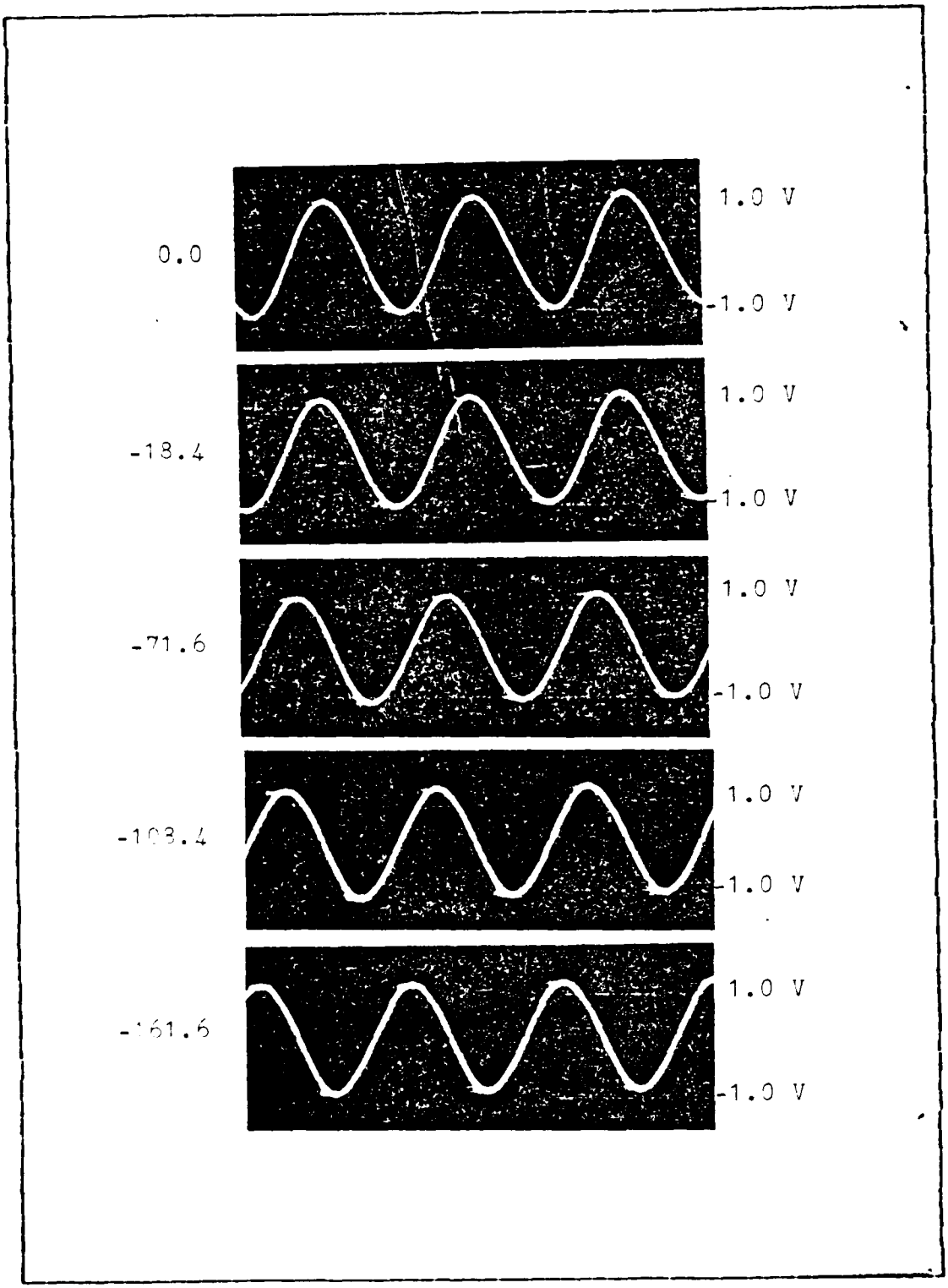

Figure 2.6 Photographs of Transmitter Output (Negative Phase)

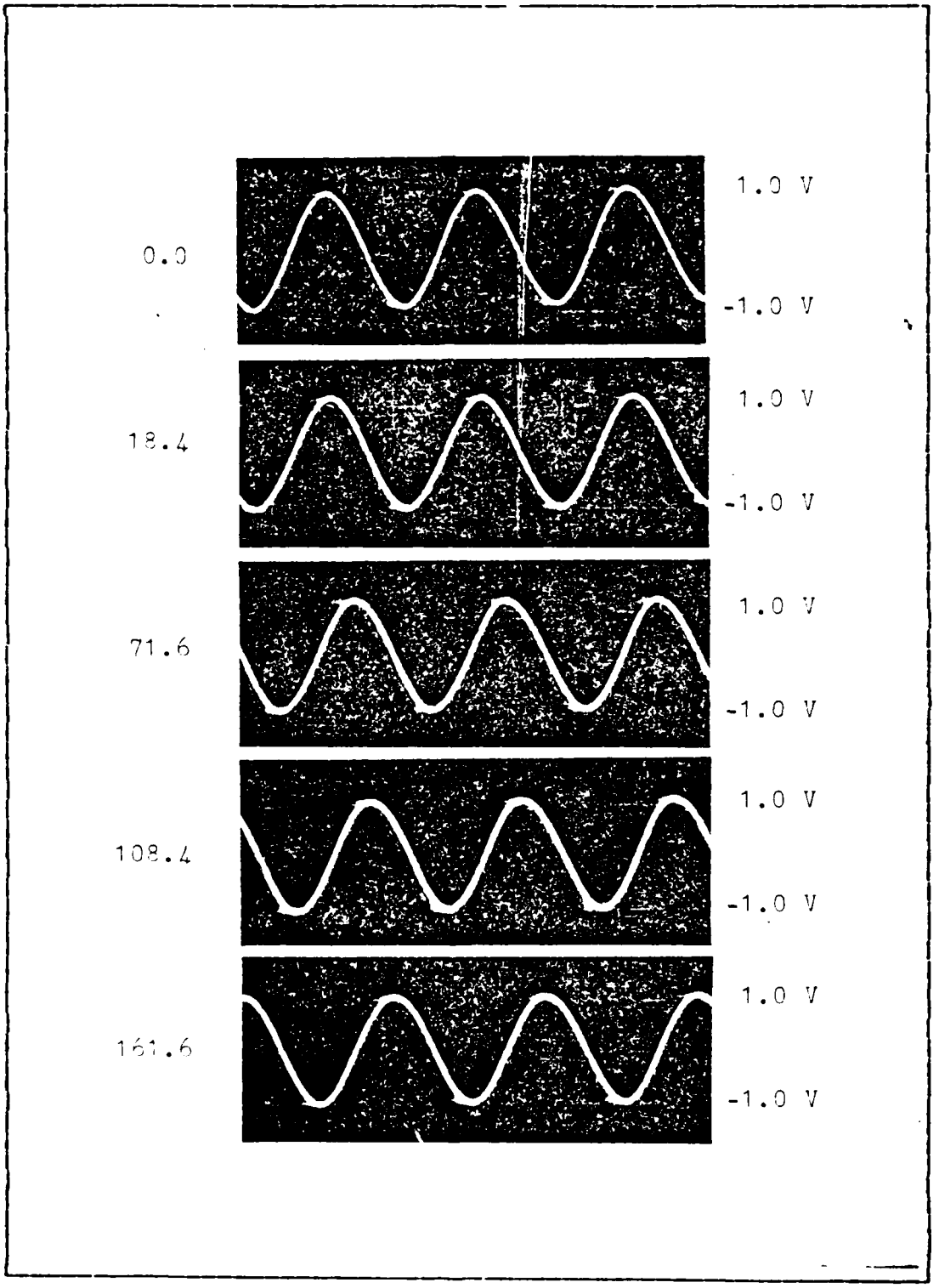

Figure 2.5 Photographs of Transmitter Output (Positive Phase)

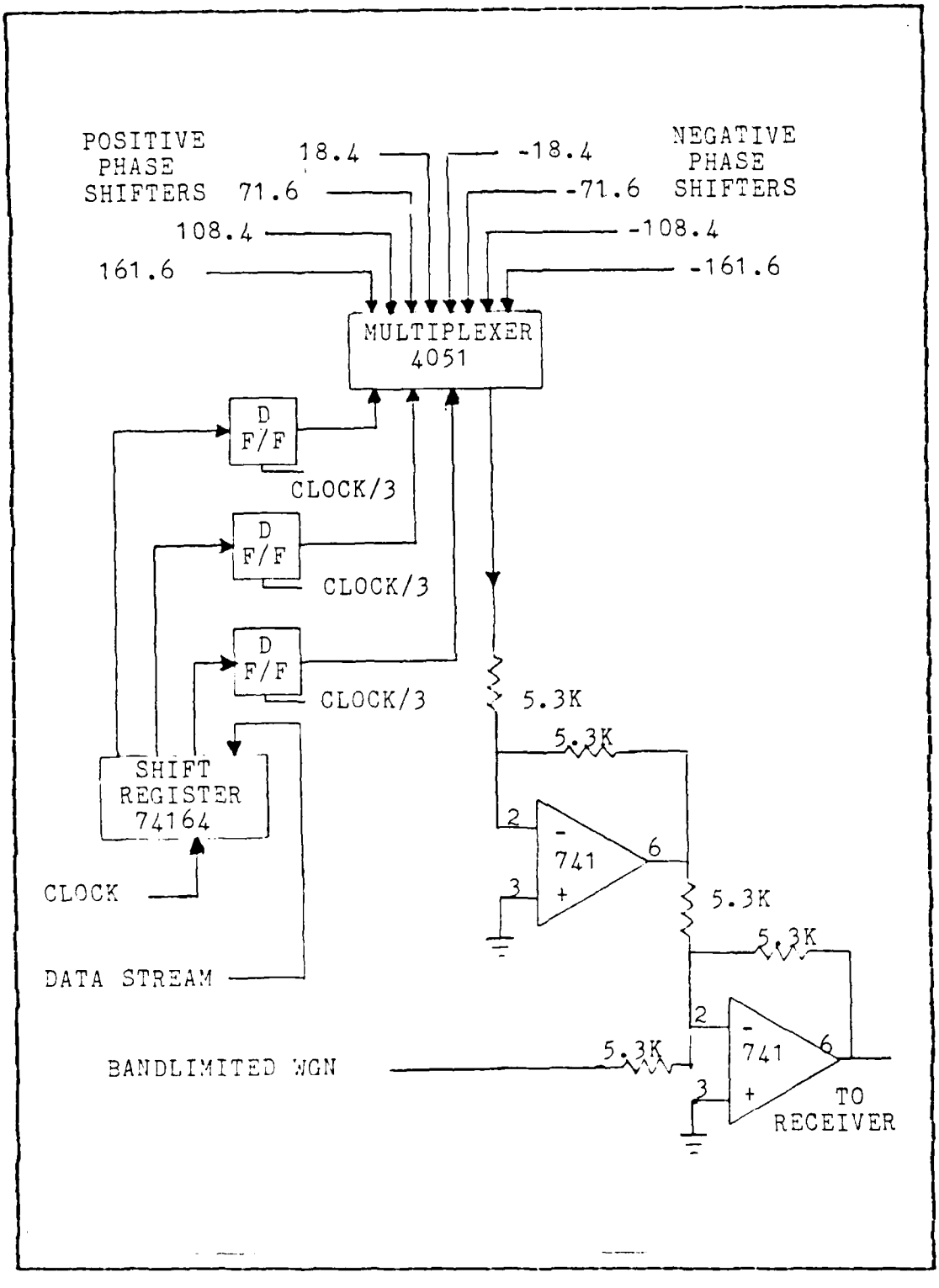

Figure 2.4 Circuit Diagram for Multiplexer, Inverter, & Summer

All phase adjustments are made using the Hewlett-Packard Gain Phase Meter Model 3575A [Ref. 1]. In addition to these eight phase shifters, two more were used to provide reference sources of 0.0 degrees (cosine) and 90.0 degrees (sine) to the receiver for coherent phase detection.

B. MULTIPLEXER

The eight phase shifted carriers are applied to a 4051 multiplexer. The desired carrier is selected by the three data bits fed to the multiplexer by three D-type flip flops. A shift register is used to set the flip flops. Two clocks are required to generate the data for the multiplexer. The data clock which reflects the data rate and the symbol clock (data clock divided by three) which clocks the data into the flip flops. Thus, the output of the multiplexer is one of the shifted carriers as selected by three bits of data. Figure 2.4 shows the detailed diagram of the multiplexer stage. Also included in the figure is an inverter and a summer. The two inputs to the summer are the inverted signal and bandlimited white Gaussian noise (WGN).

The white Gaussian noise is generated by an ELGENCO Random Noise Generator. The noise signal is passed through a biquad bandpass filter (Q=11), centered at the carrier frequency, before reaching the summer. The output from the summer is signal plus noise and is ready to be demodulated. This summing action is done tc simulate the intermediate frequency (IF) in the receiver. Figures 2.5 and 2.6 are photographs of the eight output signals generated by the transmitter.

C. GRAY CODE

The symbols (blocks) are coded so that between adjacent states the symbols differ by only one bit. This is called

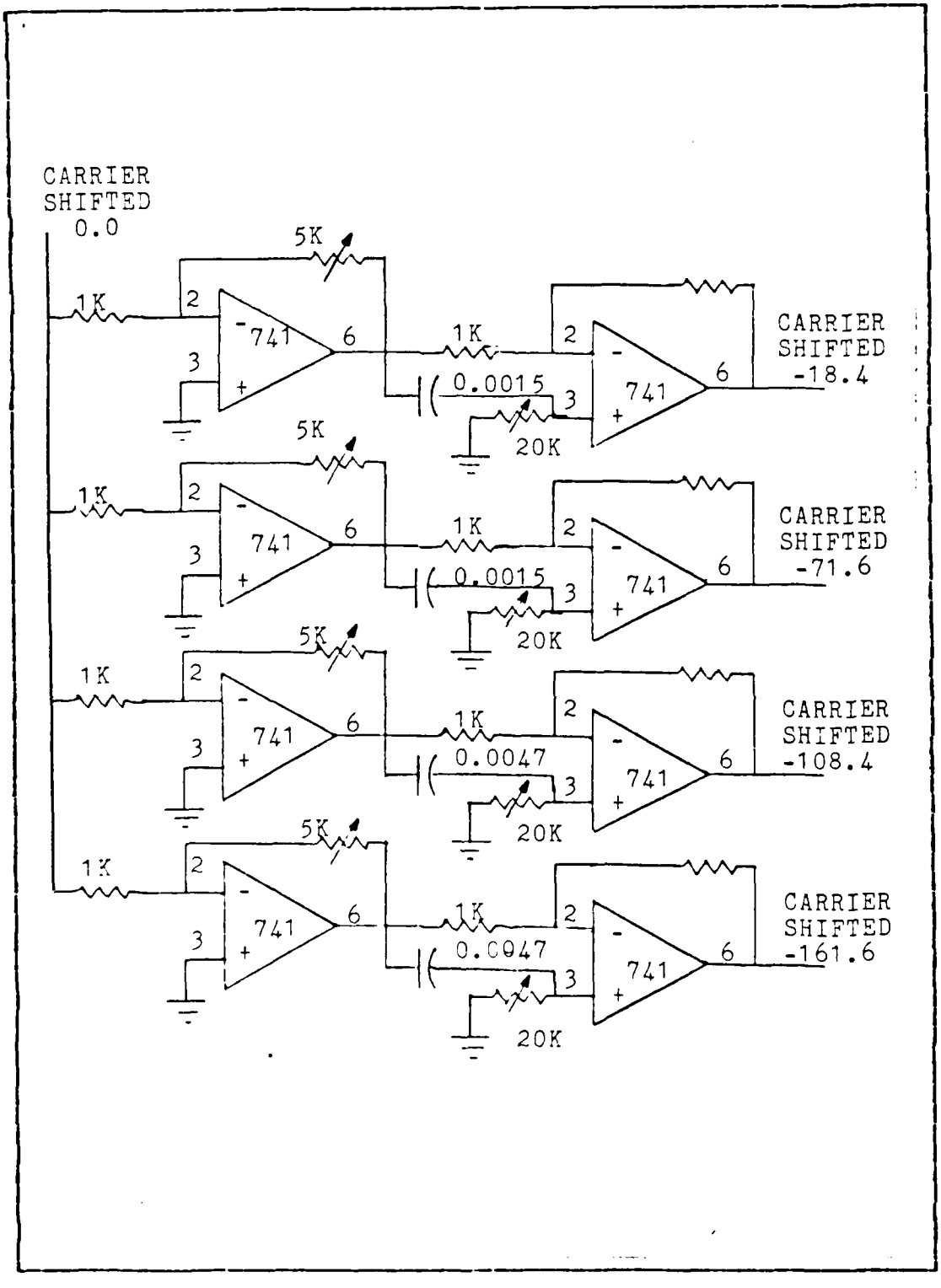

Figure 2.3 Circuit Diagram for Negative Phase Angles

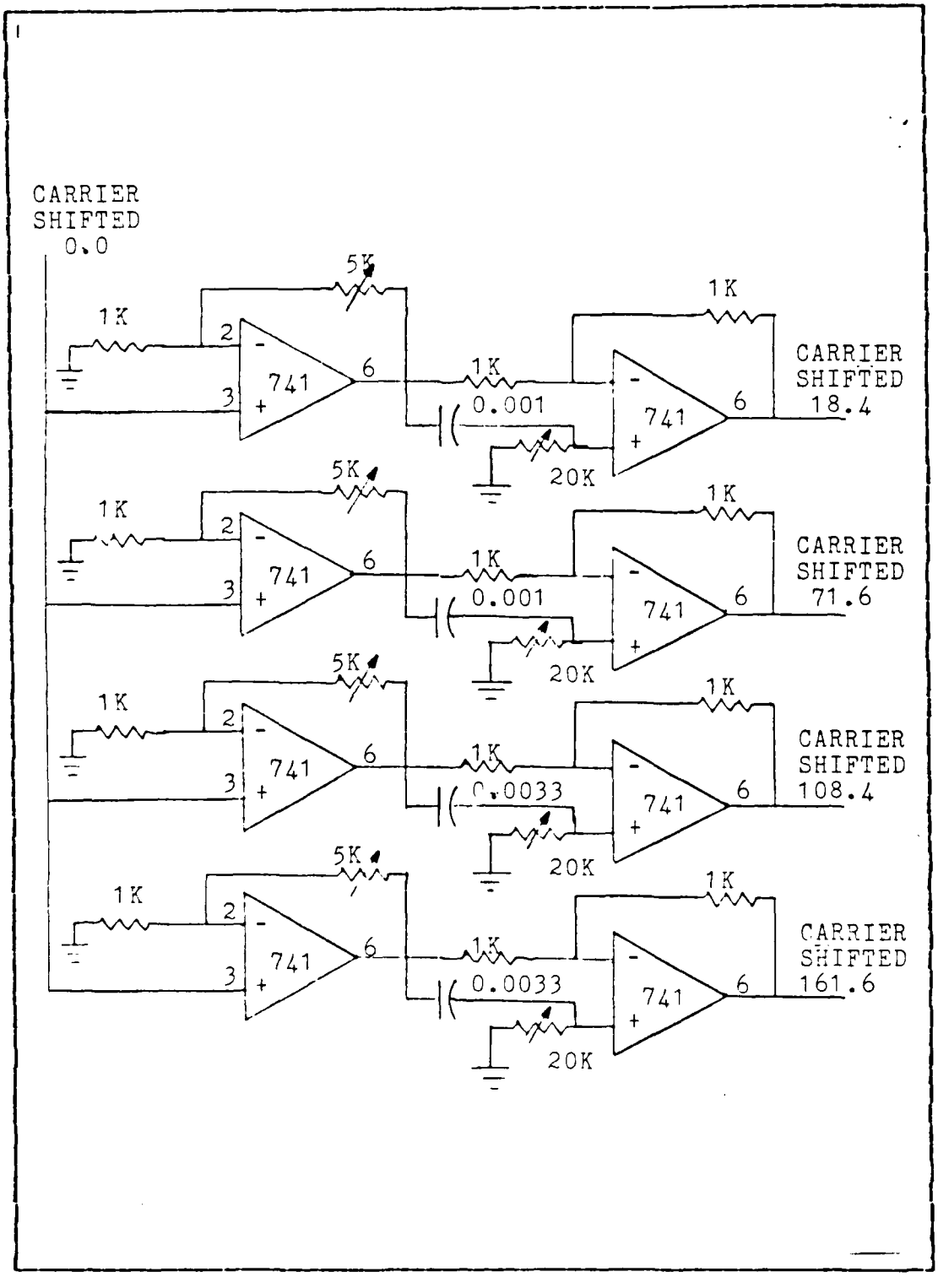

Figure 2.2 Circuit Diagram for Positive Phase Angles

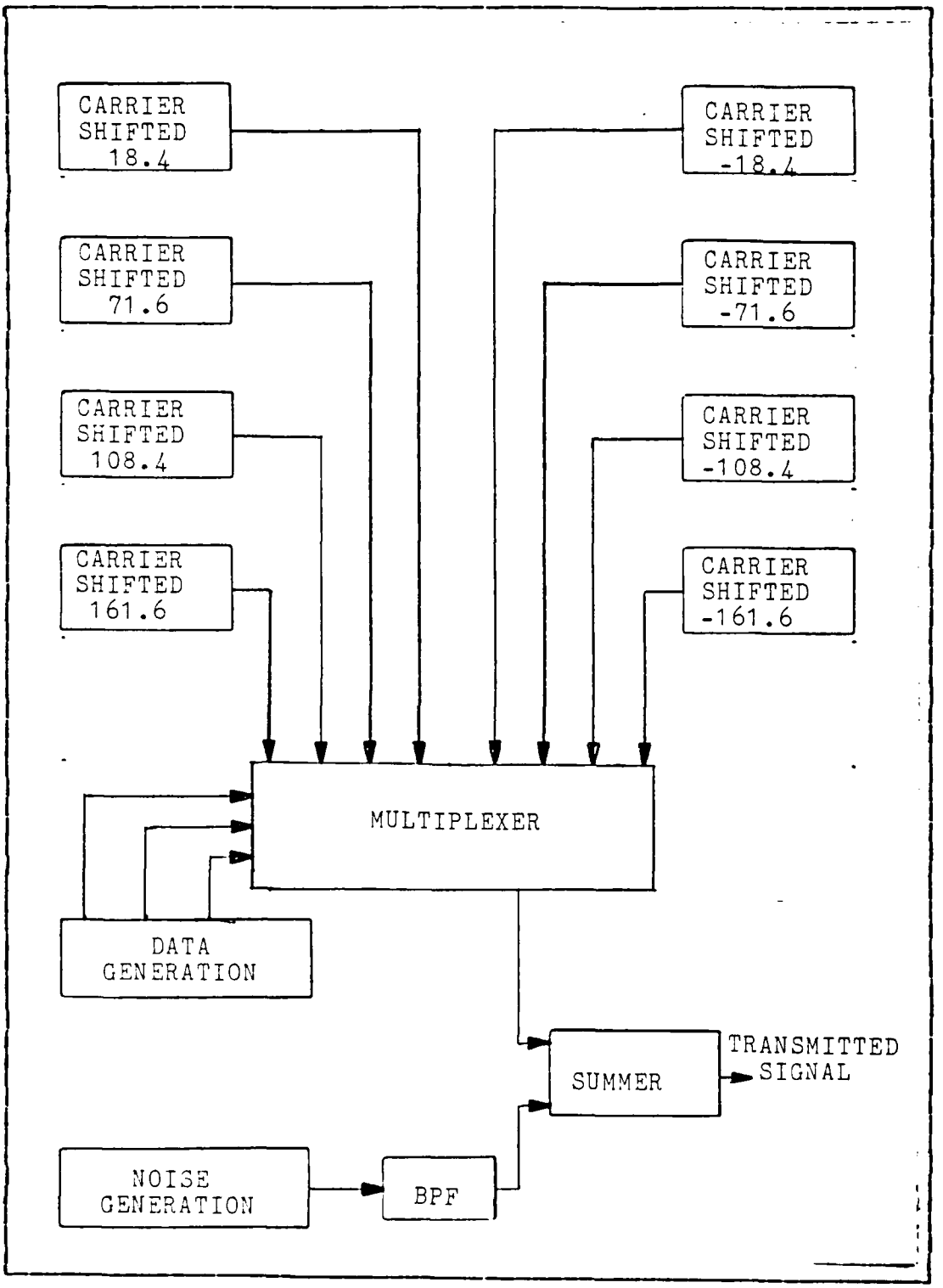

Figure 2.1 Block Diagram of Transmitter

II. TRANSMITTER

The transmitter is composed of eight phase shifters and a multiplexer. A block diagram of the transmitter is shown in Figure 2.1. Also included in the figure are the blocks for digital data generation, noise generation, and a summer (adder) to add the signal and the noise. The multiplexer is the key element of the transmitter. A given three bit symbol is used to address the multiplexer, which selects a particular one of the eight possible input sinusoids generated by the the eight phase shifters. Noise is then added to the phase modulated carrier to simulate a typical channel.

A. PHASE SHIFTERS

The transmitter requires eight phase shifters to produce eight sinusoids of the same frequency and amplitude, but different phase angles. Each phase shifter consists of two 741 op-amps. The first op-amp controls the amplitude and the second shifts the phase of the cosine carrier. Figures 2.2 and 2.3 show the generation of positive and negative phase shifts, respectively. The input for this stage is the carrier, generated by an oscillator operated at the parameters listed below.

Carrier Frequency (f) = 70 kHz

Amplitude = 2.0 volts p-p

Phase Angle = 0.0

The amount of phase change and amplitude are adjusted by the two potentiometers.

D. SUMMARY OF RESULTS

In comparing this new modulation technique (Figure 1.2) with conventional 8-ary PSK (Figure 1.1), the new method improves the noise performance by approximately 0.4 dB. This supports the basic premise of this study, that the phase angles of 8-ary PSK should be chosen so that the separation of the decision regions (voltage levels) are equal.

E. CONTENTS

The following chapters of this report consider the transmitter and the receiver built to study this method and the results and conclusions of this investigation. Chapter II describes the transmitter and includes circuit diagrams of each stage and photographs of the transmitted signal. The receiver is discussed in chapter III. Circuit diagrams of the phase detectors, matched filters, and decision logic are included along with photographs of the output of selected stages in the receiver circuitry. Chapter IV contains the detailed results of this report and recommendations for further study.

After carrier detection, the signal is processed into a usable voltage for the logic circuitry. Processing includes noise performance improvement using an integrate and dump circuit and decision circuitry using a sample and hold device and a comparator.

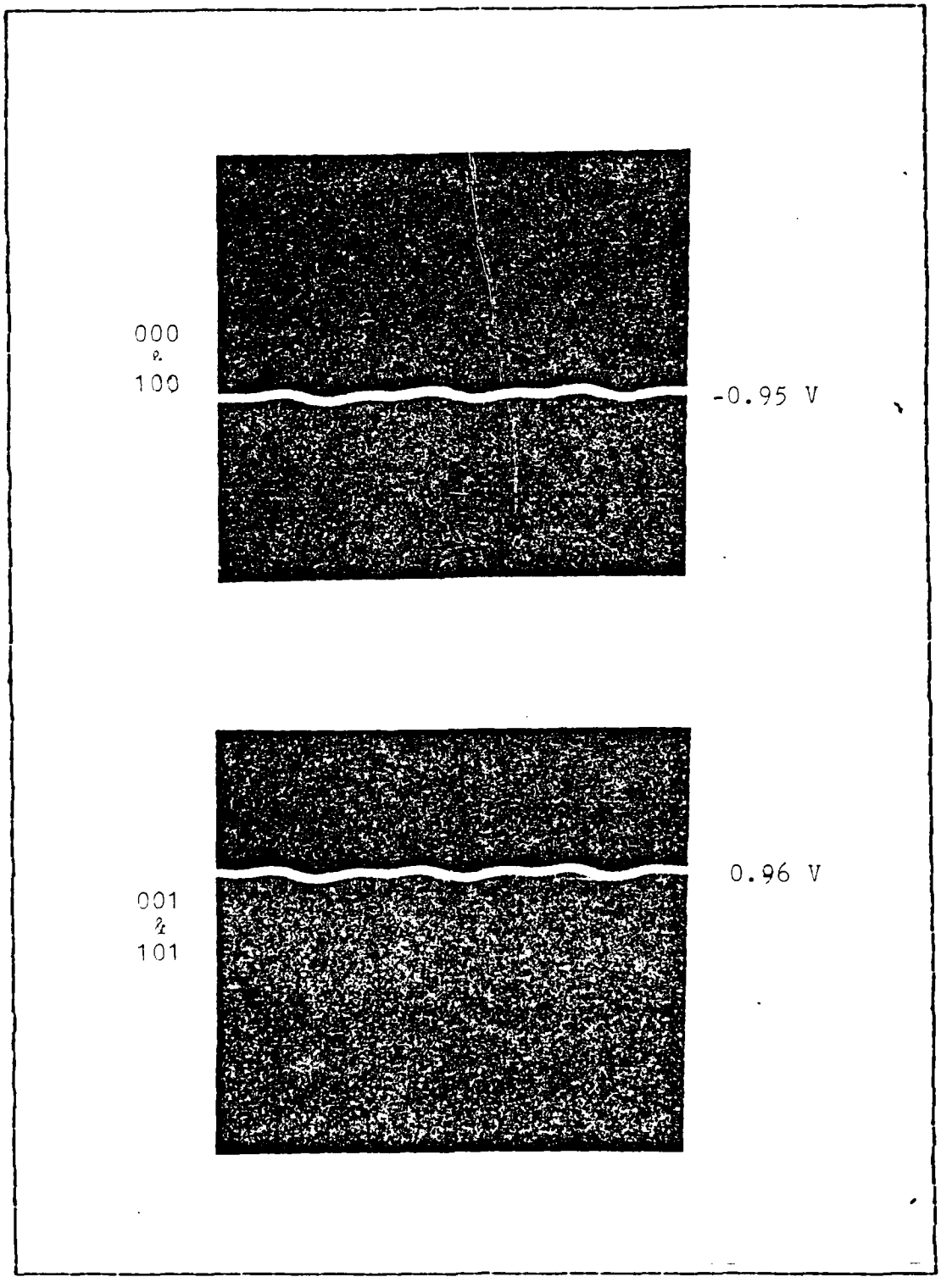

Figure 3.3 Photographs of Output of Branch #1 Phase Detector

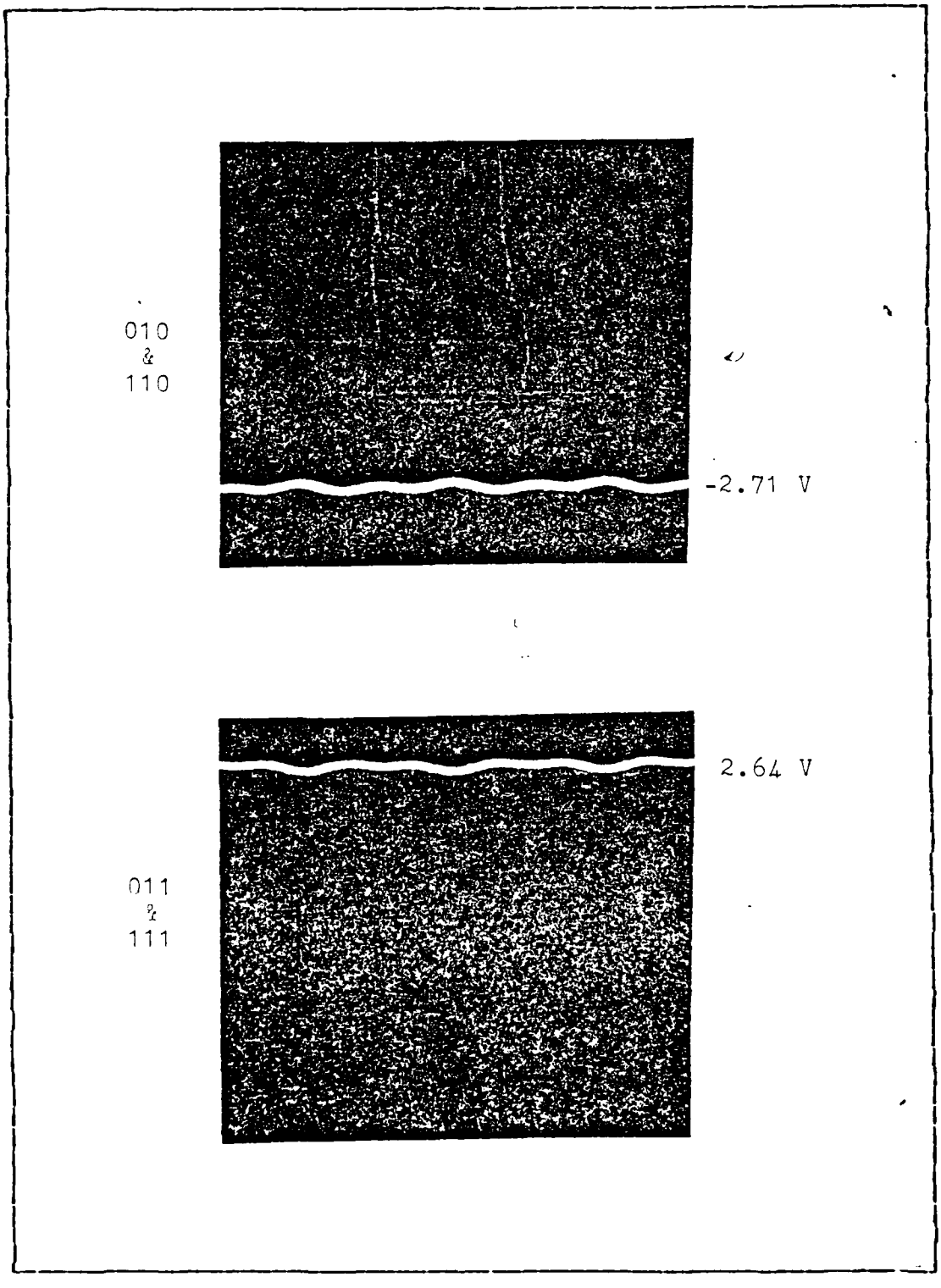

Figure 3.4 Photographs of Output of Branch #1 Phase Detector

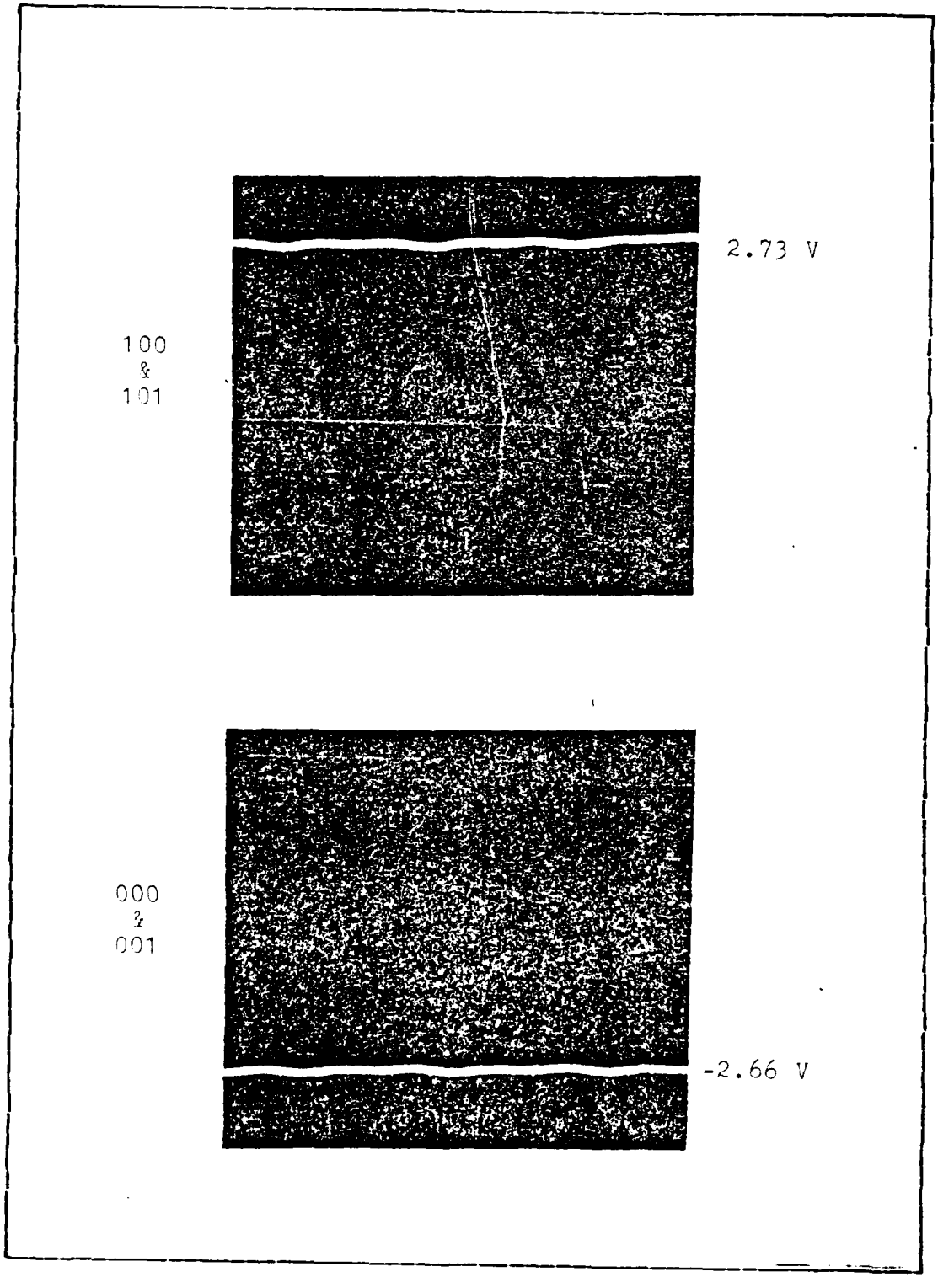

Figure 3.5 Photographs of Output of Branch #2 Phase Detector

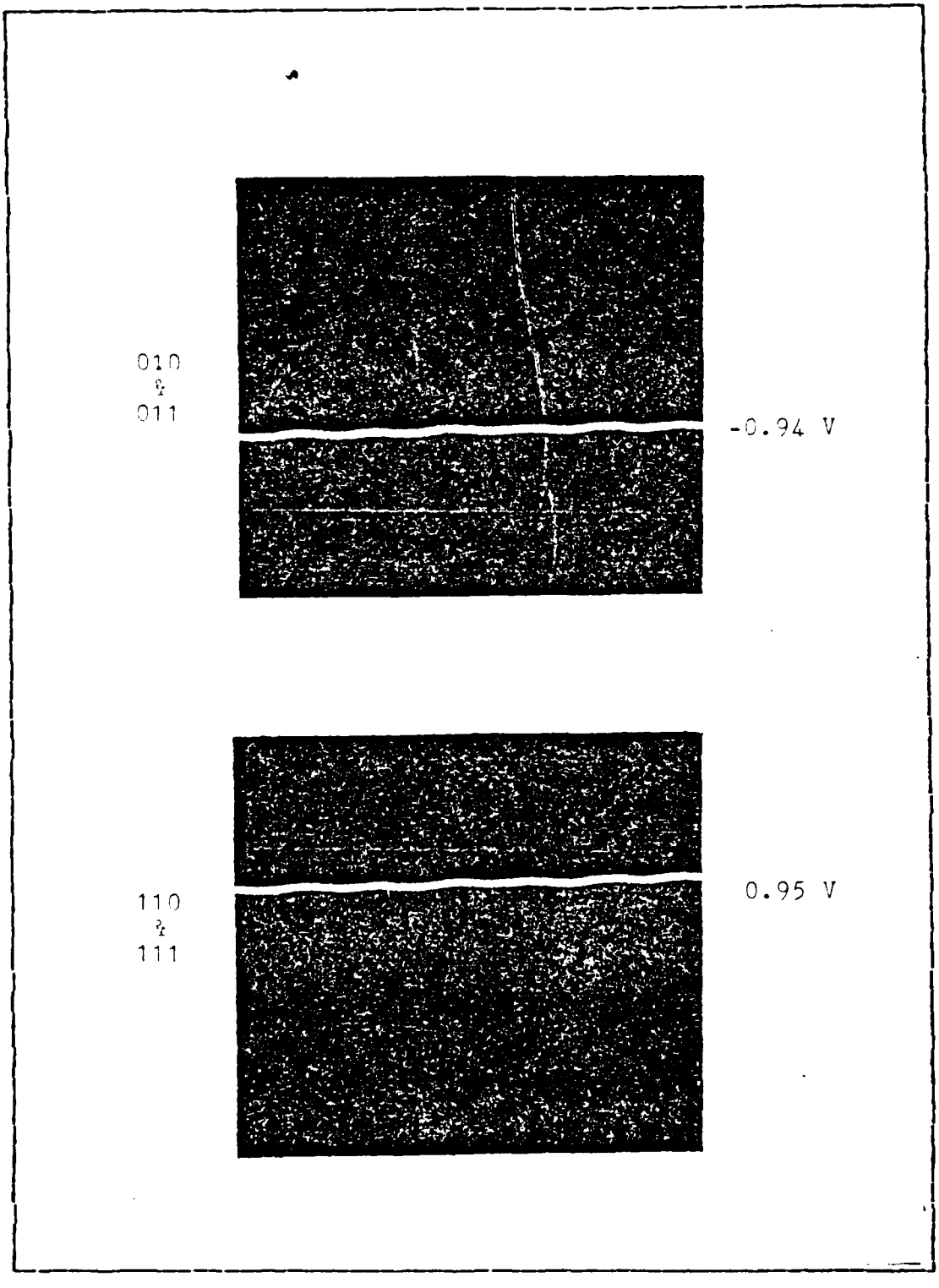

Figure 3.6 Photographs of Output of Branch #2 Phase Detector

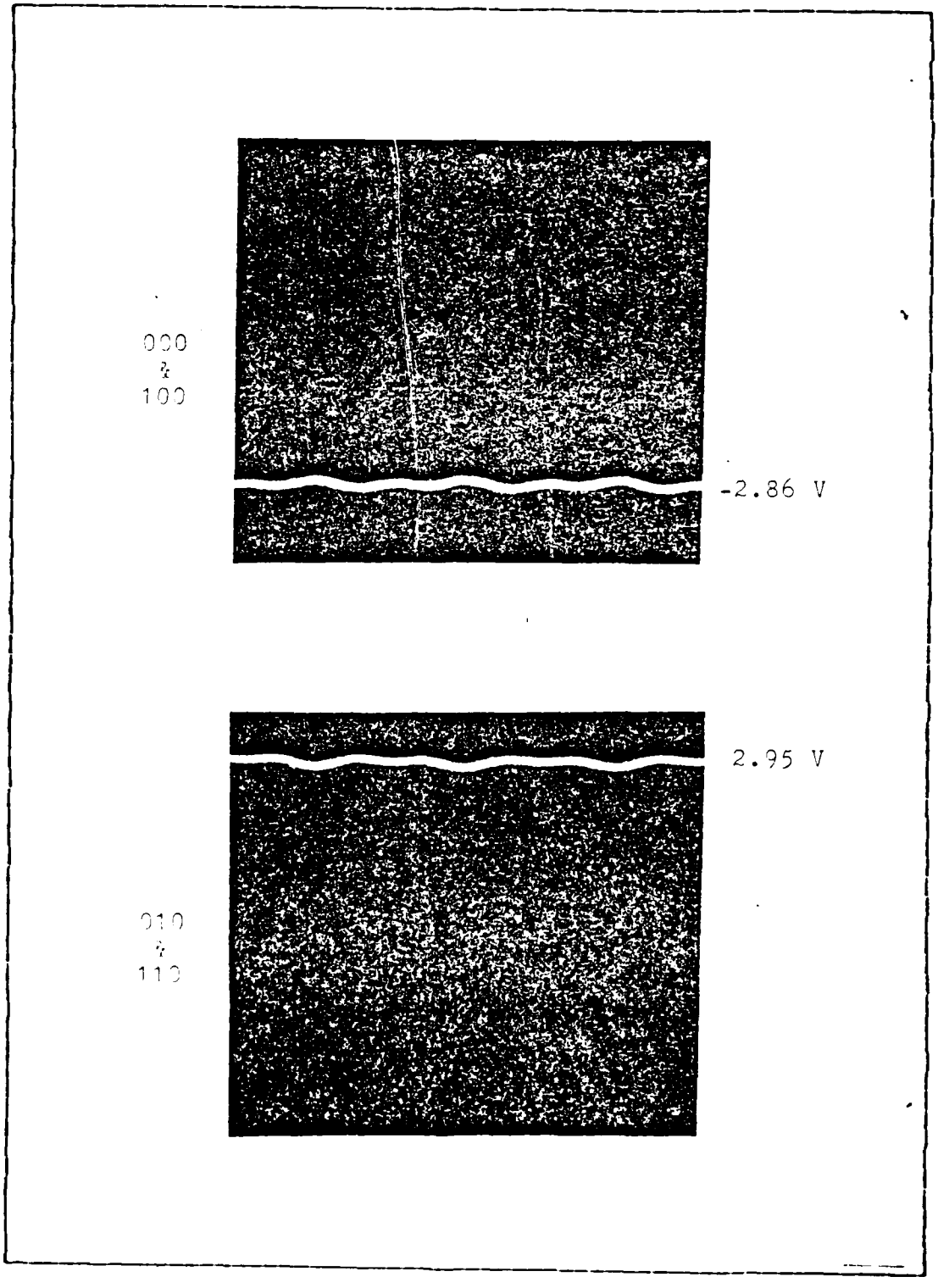

Figure 3.7 Photographs of Output of Squarer from Branch #1

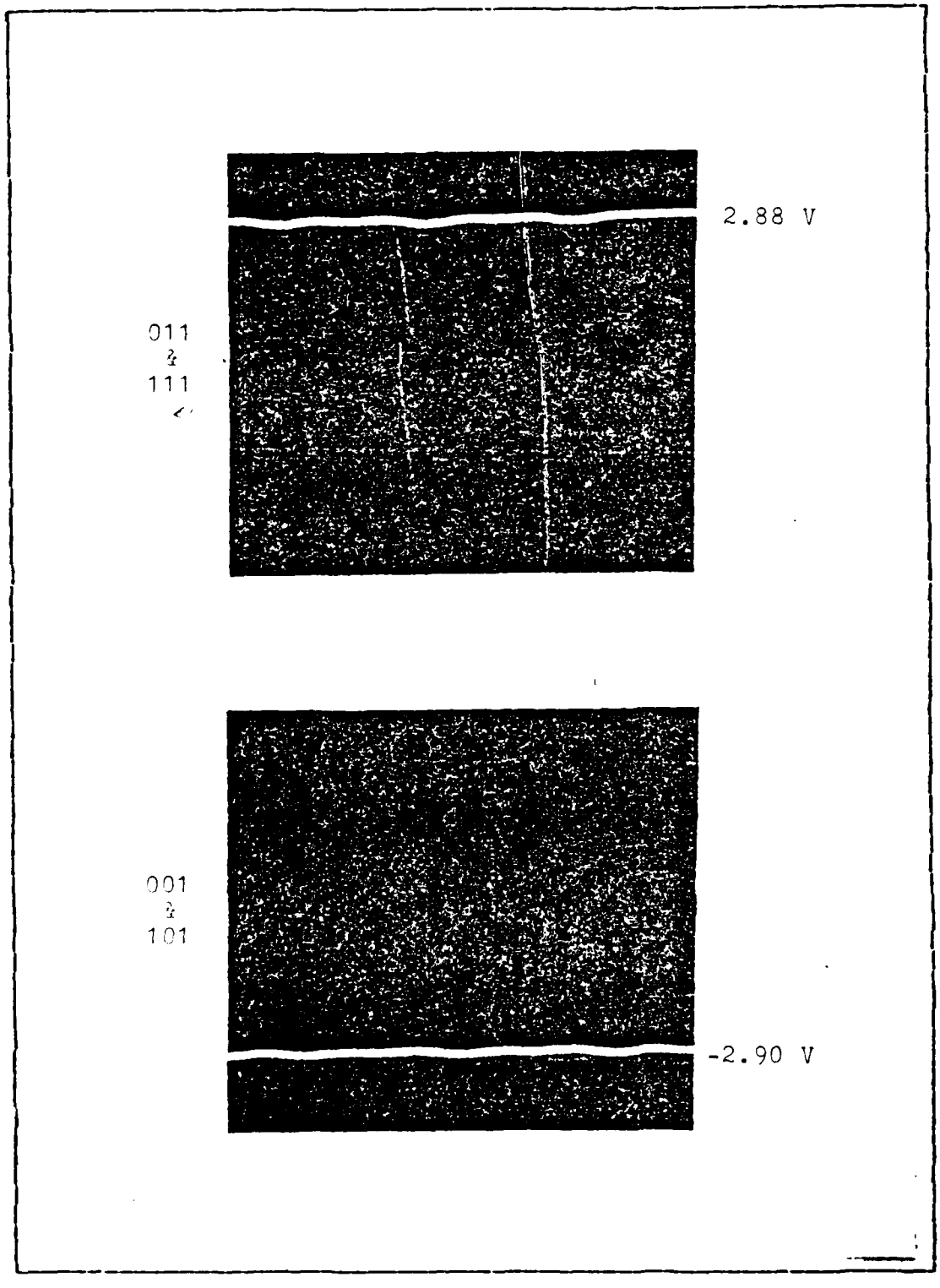

Figure 3.8 Photographs of Output of Squarer from Branch #1

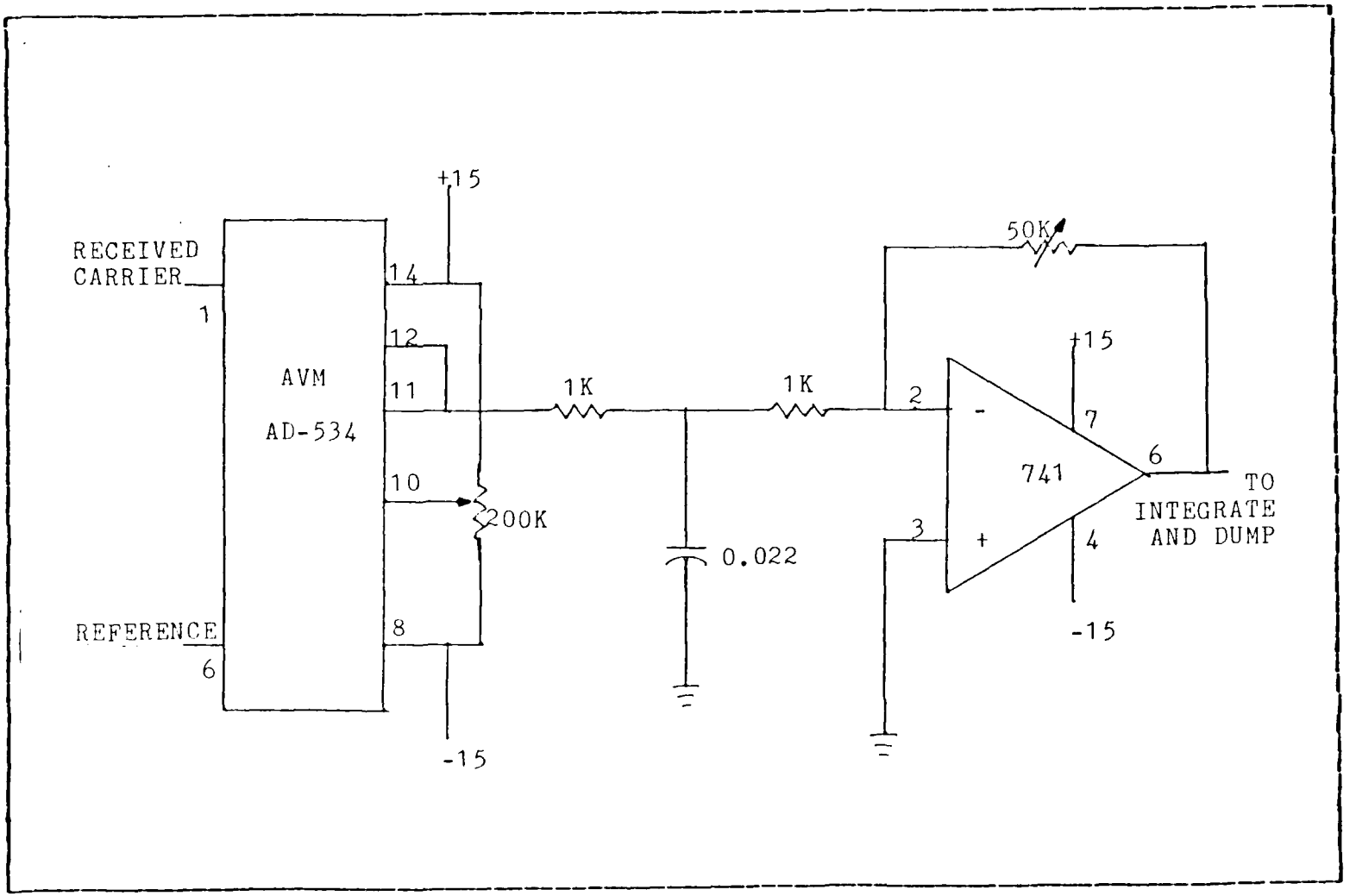

Figure 3.9 Circuit Diagram of Phase Detector

B. INTEGRATE AND DUMP

The integrate and dump circuitry is widely used to improve noise performance of receivers used in digital data systems. The circuitry integrates the demodulated signal over a symbol interval. At the end of the interval, the integrator output is sampled just prior to "dumping" or returning to zero. This reduces the effect of the noise and presents a peak value which can be used as the input to a sample and hold circuit. The two components used in the integrate and dump circuitry are the multiplexer 4051 and a 741 op-amp. The circuit is shown in Figure 3.10. The integrate and dump circuitry integrates the incoming signal and then returns to zero voltage (dumps) when the feedback circuit is shorted by the multiplexer. The clock signal which triggers the multiplexer is timed so that the dump occurs just before a new three bit block of data is transmitted. A timing diagram is shown in Figure 3.11. A photograph of the output of the integrate and dump circuitry is included in Figure 3.12. In Figure 3.12 the upper waveform on the photograph is the dump signal and the lower waveform indicates the output of a complete integrate and dump cycle. The output of the integrate and dump circuitry is a positive or a negative voltage which is translated into a logical one or zero in the next stage.

C. DECISION CIRCUITRY

The decision circuitry is composed of a sample and hold device (LF 398), a comparator (LM 311), and two buffers (741 op-amps). Figure 3.13 shows the decision circuitry. The clock for the the sample and hold device is designed to sample just before the dump portion of the previous circuit. Therefore, the desired value (the output of the integrate and dump circuit) is sampled just before its peak value and is held for the comparator. The comparator is used to

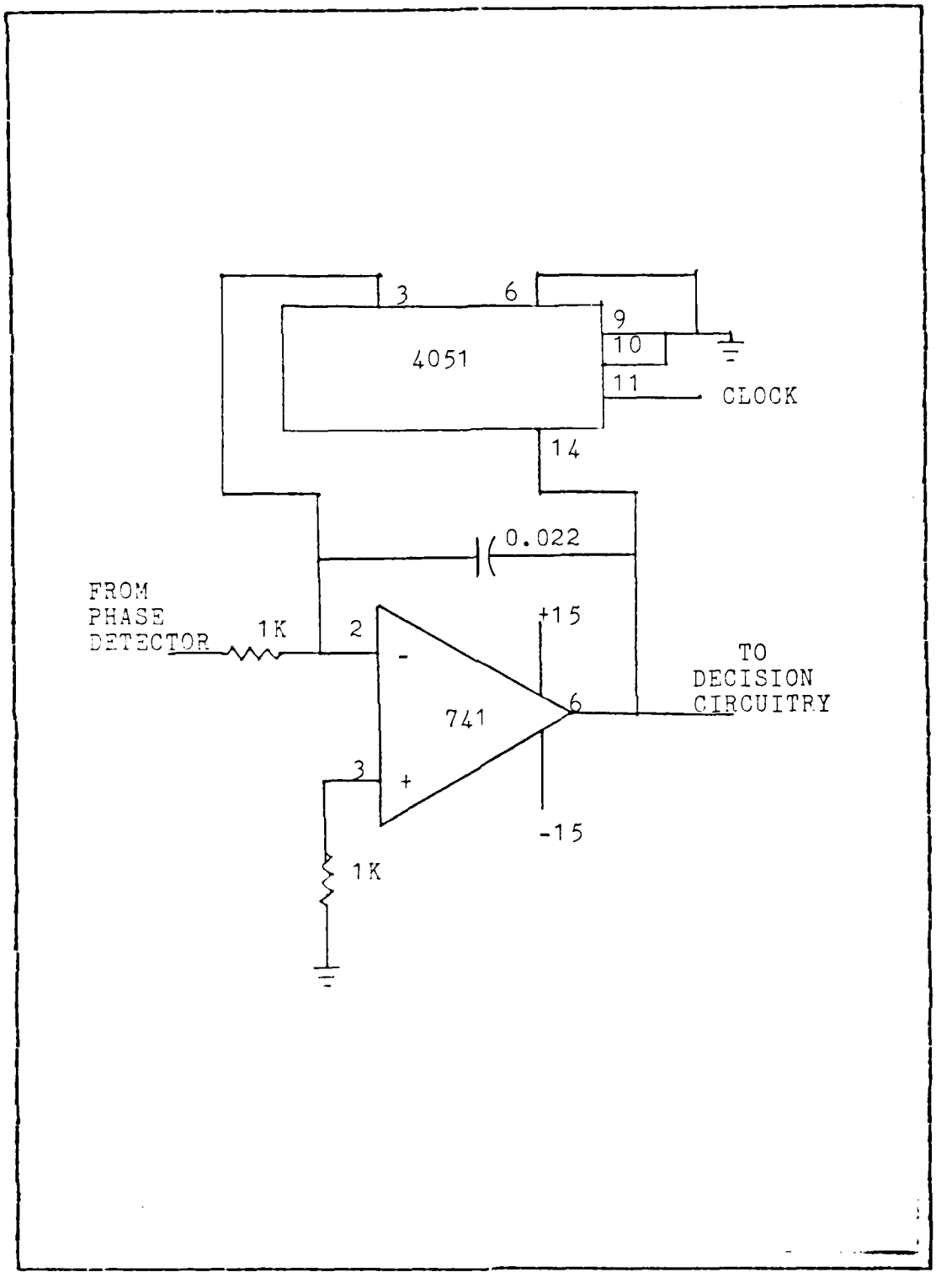

Figure 3.10 Circuit Diagram of Integrate and Dump

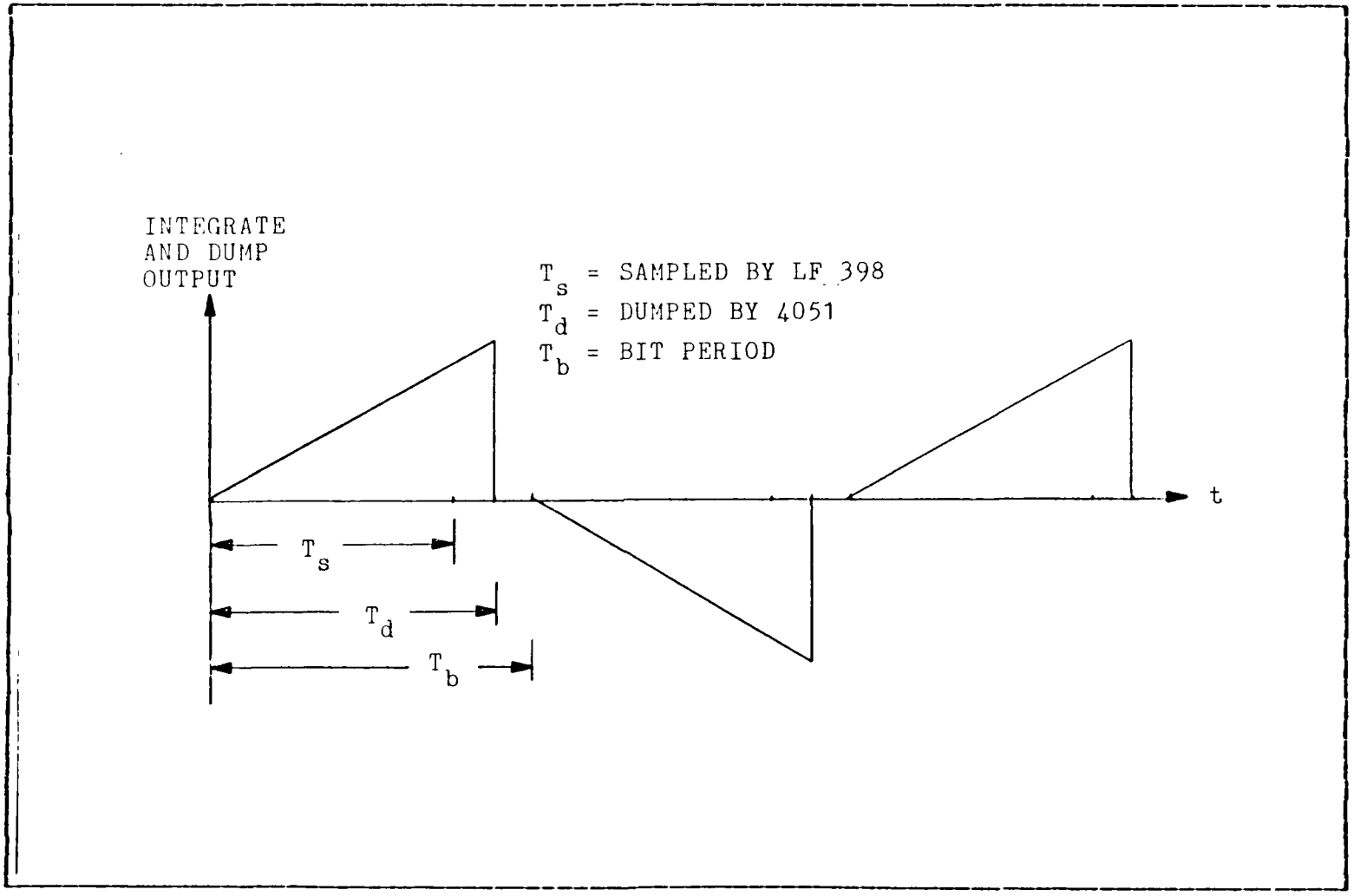

Figure 3.11 Timing Diagram of Integrate and Dump

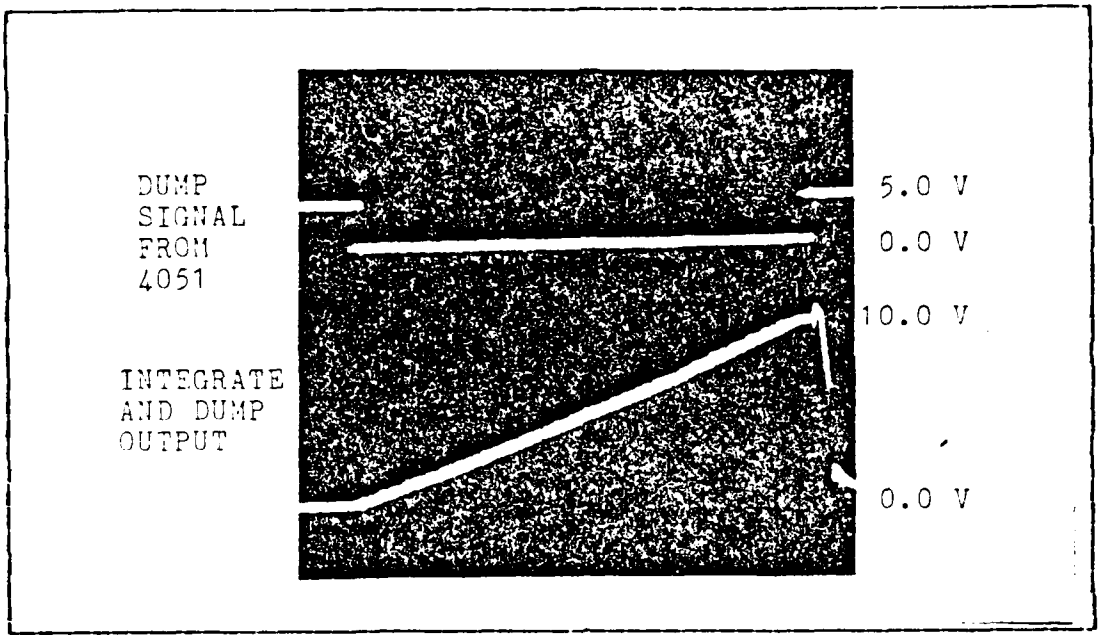

Figure 3.12 Photograph of Integrate and Dump

decide the polarity, a logical one (+5 volts) for a positive voltage and a logical zero (0 volts) for a negative voltage. This same procedure is accomplished in the recovery of the middle bit by offsetting the input to the AVM that is used as a squarer. The low magnitude value then becomes negative and the high magnitude value remains positive. The potentiometer between pins 8 and 14 of the squarer AVM is used to adjust the offset. The two buffers are used to reduce loading effects from adjacent circuitry. Recovery is now complete, and the signal is suitable for error detection by the bit error ratio (BER) detector.

D. BIT ERROR RATIO DETECTOR

The circuit is configured to allow bit error counts to be taken for each bit. Figure 3.14 is a logic diagram of this circuit. The exclusive OR gate detects the error

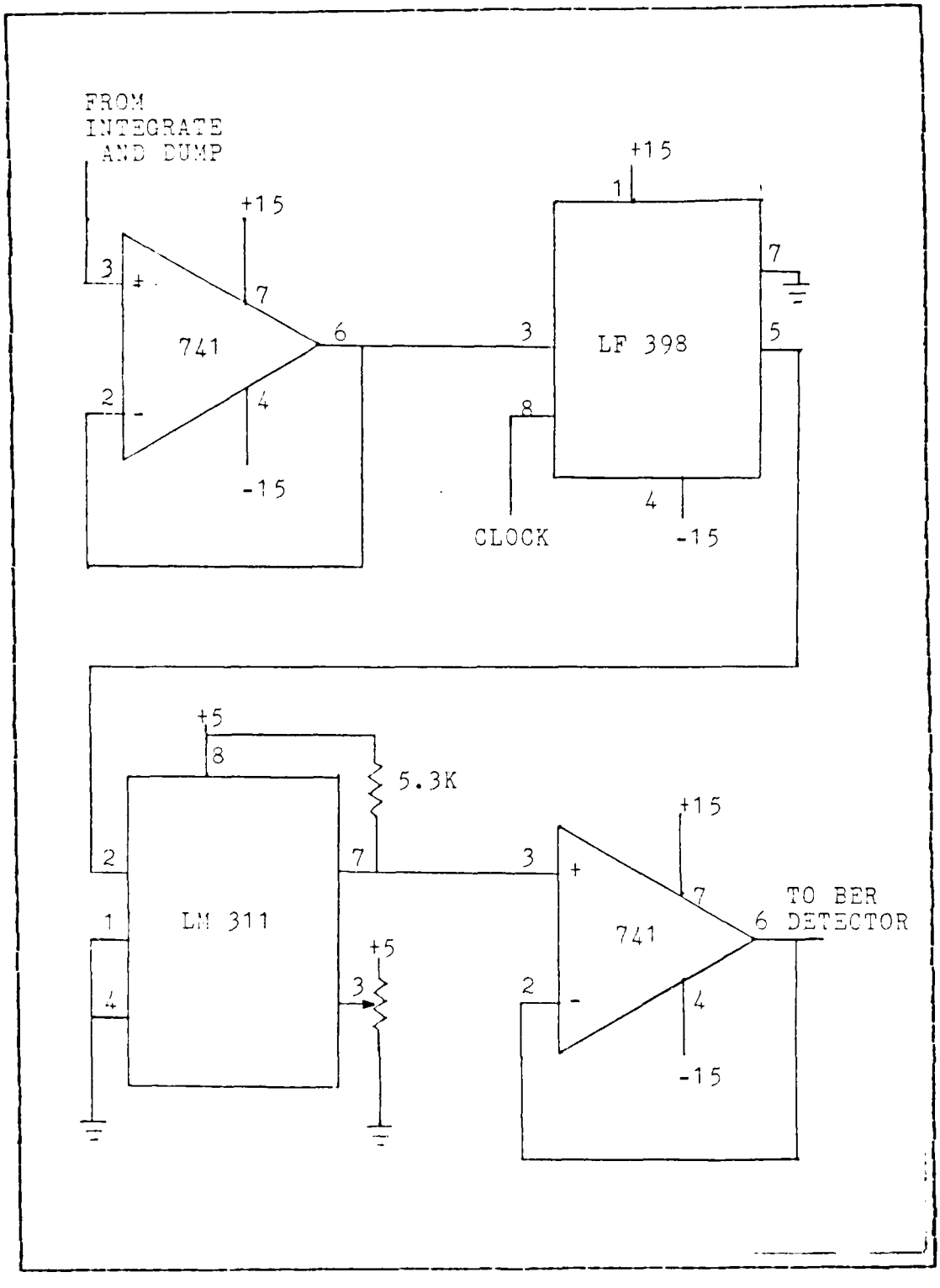

Figure 3.13 Circuit Diagram of Decision Circuitry

between transmitted and received voltage levels on a bit by bit basis. The AND gate is designed to reduce the edge effects during transition. The strobe is timed to trigger at the midpoint of the overlap of the transmit and receive pulses. A timing diagram is shown in Figure 3.15. Three counters (Hewlitt Packard Model 5302A) are used to count the errors. This method provides information on error rate for each individual bit within a symbol. The total error count is the sum of all three counters. The circuit is now ready for testing and the results are contained in the next chapter.

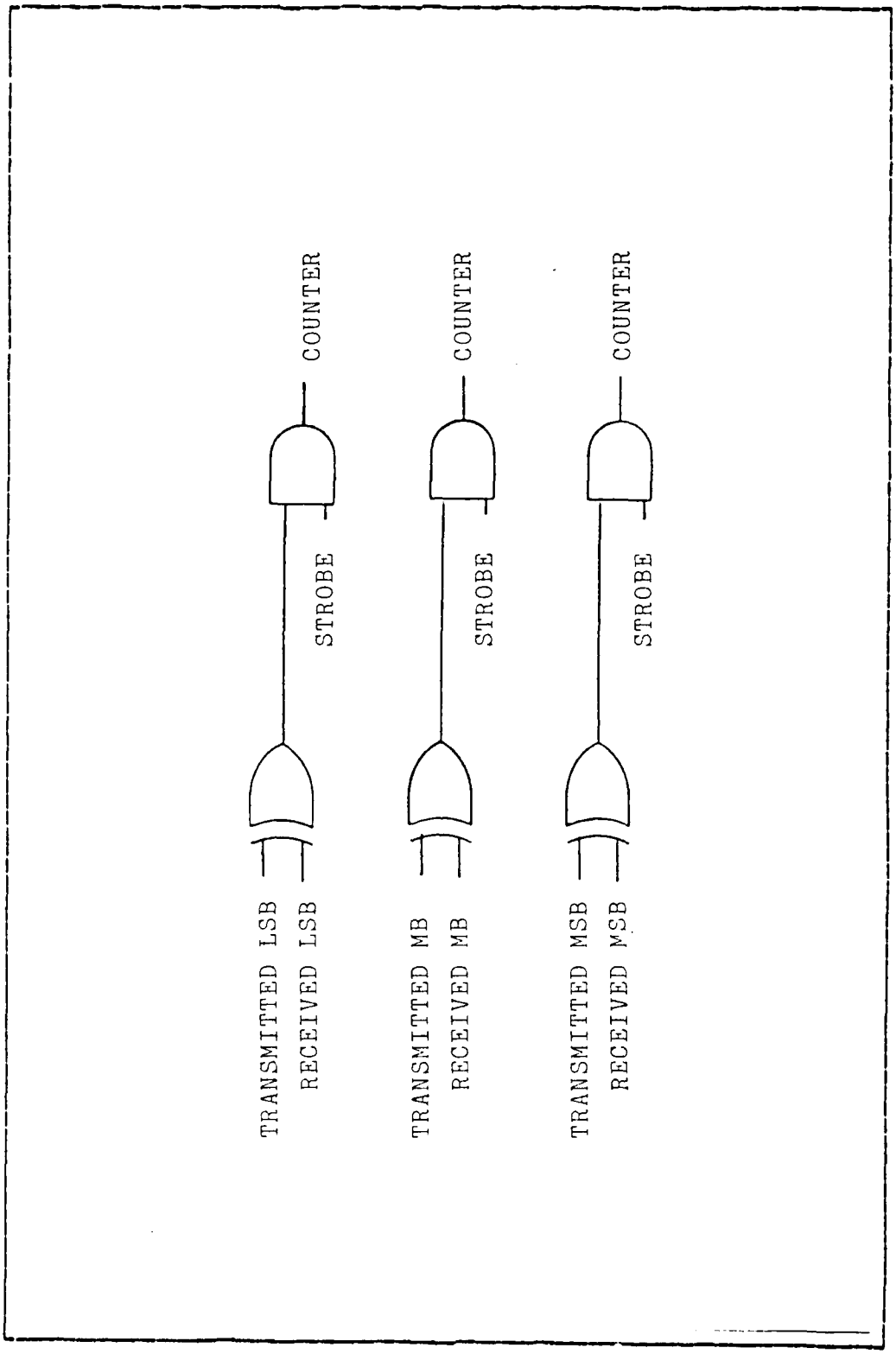

Figure 3.14 Logic Diagram of Bit Error Ratio Detector

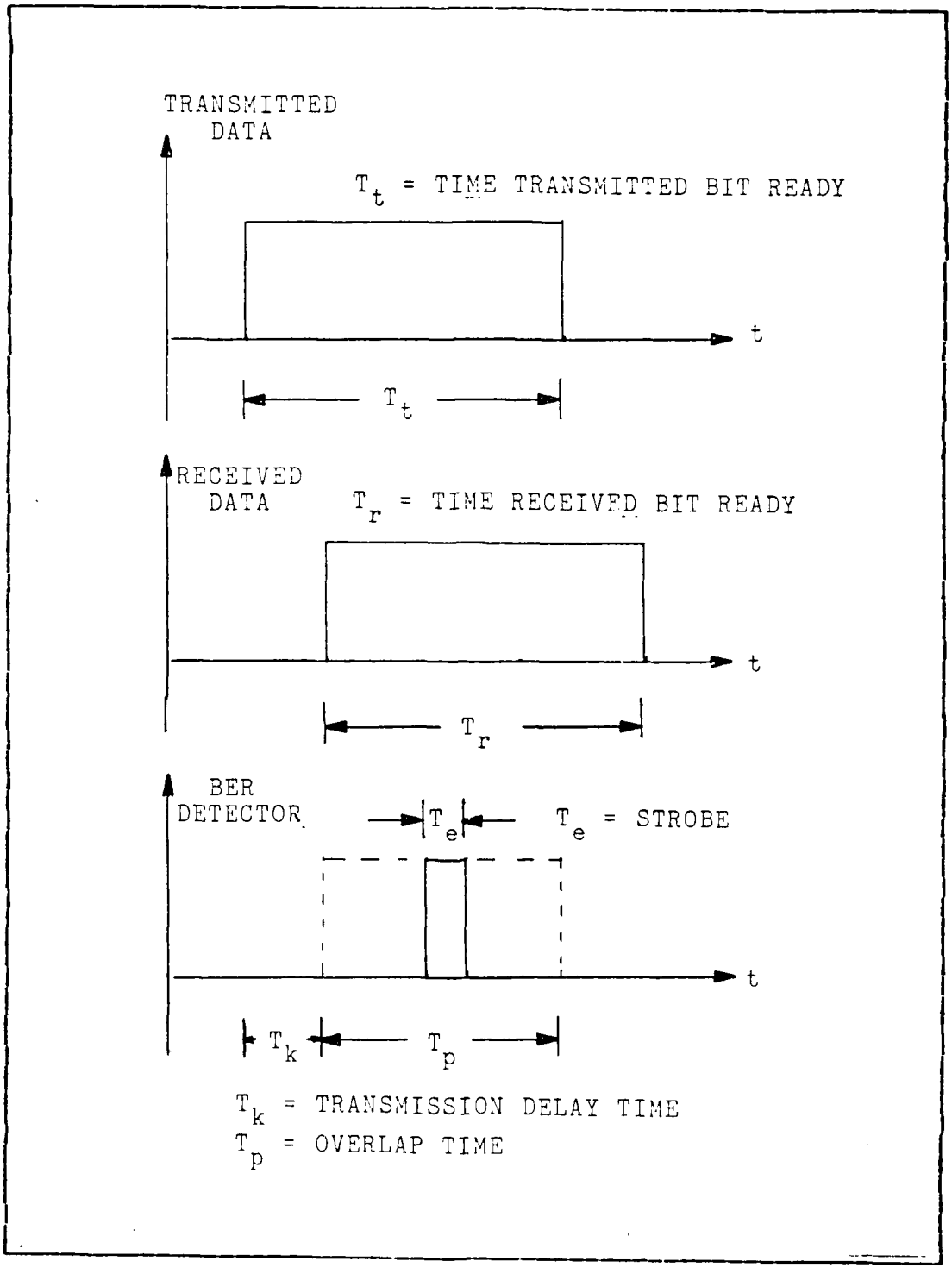

Figure 3.15 Timing Diagram of Bit Error Ratio Detector

IV. RESULTS AND CONCLUSIONS

The results of the testing of this communications system are compared with experimental results of 8-ary PSK. The signal to noise ratio (SNR) in dB versus the probability of error curves are shown in Figure 4.1.

A. THEORY

The standard values for 8-ary PSK are given in many communications textbooks and are called the "waterfall curves" (SNR vs. Probability of Error). These waterfall curves can be used to compare different communications systems. The analysis of finding the probability of error for 8-ary PSK uses the phasor diagram in Figure 1.1. A decision region is established around each phase angle (θ) as shown in Figure 4.2. Thus a decision error is made if the noise causes the phase to fall outside of the range

$$\theta - \pi/8 < \theta < \theta + \pi/8$$

This is the method adopted by most textbooks [Ref. 3]. This analysis assumes that the receiver consists of eight phase detectors and that the decision logic selects the phase detector with the largest output. Probability of error curves which are based on this analysis then cannot be compared with receivers that use two phase detectors such as the one tested in this report. Further, the decision logic in this receiver decodes all three bits simultaneously and a decision matrix is not necessary to recover the data bits. These differences will affect the probability of error analysis which is a topic for further study.

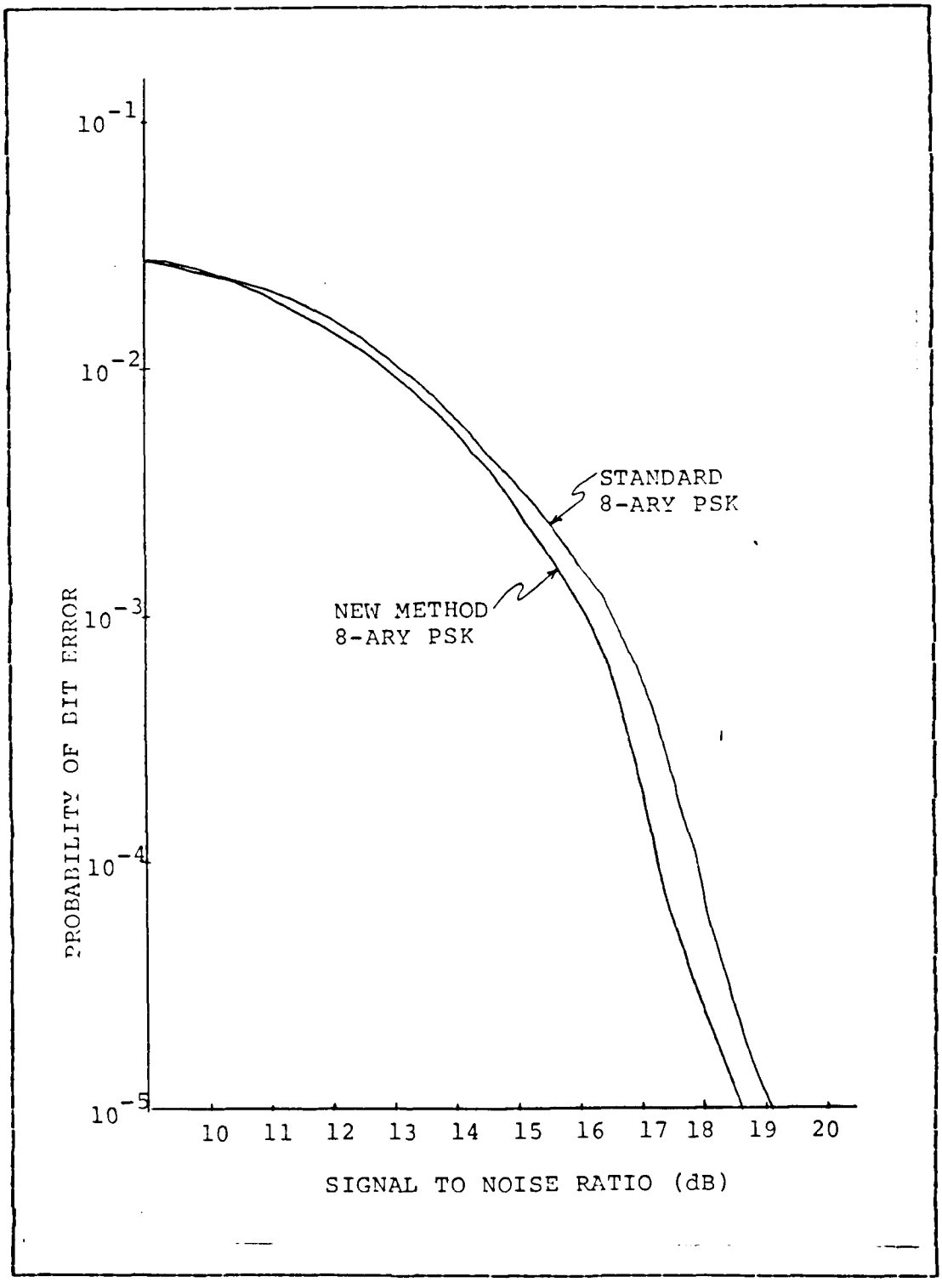

Figure 4.1 SNR vs. Probability of Error 8-ary PSK Systems

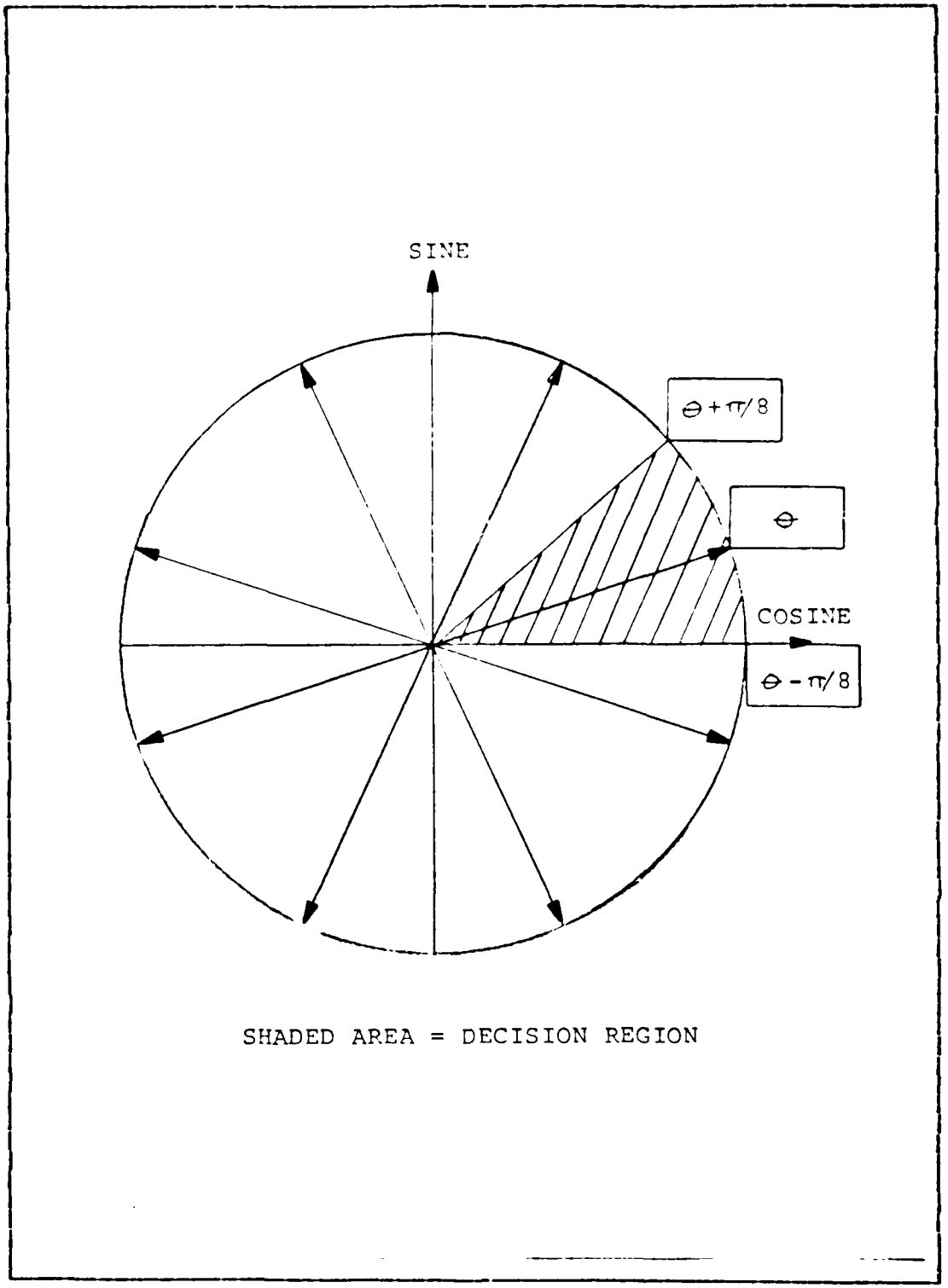

Figure 4.2 Decision Region Surrounding a Phase Angle

B. STANDARD 8-ARY PSK

To compare the results of this study with standard 8-ary PSK the transmitter was adjusted to transmit the phases as shown in the phasor diagram in Figure 1.1. The phasor diagram shows eight phases equally spaced. The receiver was not changed except to optimize the threshold levels resulting from the phase changes. The data for this system is shown in Figure 4.1 for comparison with the new modulation technique.

C. RESULTS

The results of the new modulation technique are also shown in Figure 4.1. This technique shows an improvement of approximately 0.4 dB over convertional PSK.

D. CONCLUSIONS

The results of the testing of this communications system support the concept stated in the introduction. Decision regions should be spaced equally, and because decisions are based on voltage (not phase), this new modulation technique gives a measurable improvement in noise performance.

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